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A Simulation-Driven Experiential Learning Framework for Teaching Ultra-Low-Power Analog Design Using Class-AB Recycling Folded Cascode OTAs

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***Abstract*— This paper discusses the design and analysis of an ultra-low-power Class-AB Recycling Folded Cascode (RFC) Operational Transconductance Amplifier (OTA) for high-density biomedical sensing interfaces implemented with 45 nm CMOS technology. The proposed design tackles the trade-off between power use and driving capability found in traditional Class-AB operation. To address this issue, the RFC core features a dynamic Class-AB boosting mechanism, which improves the slew rate performance without significantly increasing quiescent current. The design method relies on the gm/ID approach, allowing for optimal transistor sizing in the subthreshold region. Furthermore, this methodology serves as a comprehensive educational case study for instructing students on subthreshold device optimization in modern nanometer regimes. This maximizes transconductance efficiency while meeting strict power limits. This makes the proposed OTA especially suitable for battery-powered and energy-limited biomedical applications. Simulations show that the OTA achieves a DC open-loop gain of 75.73 dB, a Common Mode Rejection Ratio (CMRR) of 136.36 dB, and a phase margin of 84.02° while driving a capacitive load of 20 pF. The circuit has a positive slew rate of 0.024 V/µs, with total power consumption of just 337.5 nW from a 1 V supply. Additionally, the design demonstrates strong robustness across variations in process, voltage, and temperature (PVT), ensuring reliable operation in real-world conditions. Thanks to its low power consumption, high gain, and stability, the proposed OTA is ideal for low-frequency bio-signal acquisition systems, such as wearable and implantable medical devices, where energy efficiency and signal quality are essential.**

***Keywords*— 45 nm CMOS, Biomedical applications, Class-AB, Common Mode Rejection Ratio, gm/ID methodology, Recycling Folded Cascode.**

I. INTRODUCTION

The rising number of wearable health monitoring systems and implantable medical devices is prosperous an unprecedented requirement for ultra-low-power analog front-ends (AFEs) (Garde, 2018), (Sansen, 2012), (Lee, 2014), (Li et al., 2026). Simultaneously, there is a growing demand for pedagogical tools that are practice-oriented and connect the gap between theoretical analog circuit design and its implementation in real life biomedical applications. The work at hand proposes a simulation- driven experiential learning framework for ultra-low-power AFEs design as an innovative attempt to solve both challenges.

In this context, AFE design becomes a contextualized instructional setting where students experience firsthand the realities of contemporary engineering constraints such as low signal amplitude, noise immunity, and tight power budgets. Physiological signals, such as ECGs and EEGs, as well as neural spikes (Moosaei, 2025), (Harrison, 2003), (Harrison, 2008), are inherently low amplitude and low frequency, presenting a challenging design task (Gosselin, 2011). For designing interfaces for such signals, high open-loop gain (Kasipogula, 2024), low input-referred noise and high common-mode rejection ratio (CMRR) are required (Gregorian, 1986). Requirements of these are integrated into a guided simulation workflow, allowing learners to assess circuit performance in cycles and build intuition regarding their sensibility to design parameters.

At the heart of the proposed way of teaching this subject is having students systematically explore design trade-offs. Due to the necessity for AFEs operating in a sub-microwatt regime must exist for more extended periods or use energy harvesting, students and practitioners need to balance gain against bandwidth and power consumption. The core instructional module as a building block is the operational transconductance amplifier (OTA). Learners get hands-on training on how to balance circuit performance under realistic constraints through progressive design tasks and simulation-based analysis (Carusone, 2011), (Kinget, 2013), (Sedra, 2015), (Baker, 2019), (Franco, 2002).

The framework presents OTA architectures from easy to more complex in order to allow for scaffolded learning. Firstly, the folded cascode OTA is investigated because of the high output swing and wide common-mode range of input (Bult, 2002). This flaw in low-power operation opens the door to recycling folded cascode (RFC) topology (Assaad, 2009), that uses current reuse techniques that improve transconductance efficiency and gain-bandwidth product, without increasing power consumption (Dabas, 2022). This progression enables learners to directly observe how architectural innovations respond to pragmatic challenges while reinforcing design-oriented practices.

Based on this background, we study an advanced case in the proposed work using a Class-AB RFC OTA realized in 45 nm CMOS technology (Galan, 2007), (Loikkanen, 2010), (Pandey, 2024). In contrast to traditional Class-A RFC designs that suffer from output current limitation under constant biasing (Garde, 2018), (Razavi, 2029), the modulation of Class-AB operation provides dynamic current boosting for better transient response at a fraction of quiescent power. This design acts as both a technical contribution and the capstone learning module, showing how biasing strategies influence speed–power trade-offs.

The design methodology relies on gm/ID based approach which is a great framework to use in education as it intuitively describes the device operation at inversion regions (Chen et al., 2024), (Silveira, 2002), (Jespers, 2017). The sub-threshold regime exposes students to energy-efficiency principles of design and noise–power trade-offs. Achievement: The last OTA delivers high gain, strong CMRR, and stable operation driving a 20 pF load with 337.5 nW power consumption.

Two main contributions can be found in this paper:

1. Simulation-Based Approach over Scaffolded Learning to teach Ultra-low-Power Analog design, and
2. The Class-AB recycling folded cascode OTA being implemented as a high-performance, yet pedagogically effective design example

Section II introduces the educational model and learning framework, Section III describes the OTA architecture, Section IV exhibits simulation results and their teaching implications, and Section V summarizes this paper.

II. Design Methodology and Transistor Sizing

The proposed ultra-low-power Class-AB RFC OTA is implemented using 45 nm CMOS technology. In modern deep submicron processes, traditional square-law models become increasingly inaccurate due to the dominance of short-channel effects, velocity saturation, and carrier mobility degradation (Enz, 2006), (Enz, 1995), (Tsividis, 2011). Understanding these non-ideal effects is essential not only for advanced circuit design but also as a key learning component in contemporary analog VLSI education.

To address these challenges, the optimization of transistor aspect ratios (W/L) is carried out using the gm/ID design methodology. This approach provides a systematic and insight-driven framework for analog circuit design, making it highly suitable for both research and instructional purposes. Unlike conventional equation-based methods, the gm/ID methodology relies on normalized characteristic curves obtained from Cadence SPICE simulations, enabling designers and students to better visualize and understand the trade-offs between transconductance efficiency, current consumption, and bandwidth (Silveira, 2002), (Jespers, 2017).

The fundamental design equation used to determine the width of each transistor is given as follows:

$$W = \frac{g_m}{\left(\frac{g_m}{I_D}\right)_{\{target\}} \times \left(\frac{I_D}{W}\right)_{\{target\}}}$$

Using this relationship, the circuit is sized to meet the stringent power budget of 337.5 nW while driving a substantial 20 pF load.

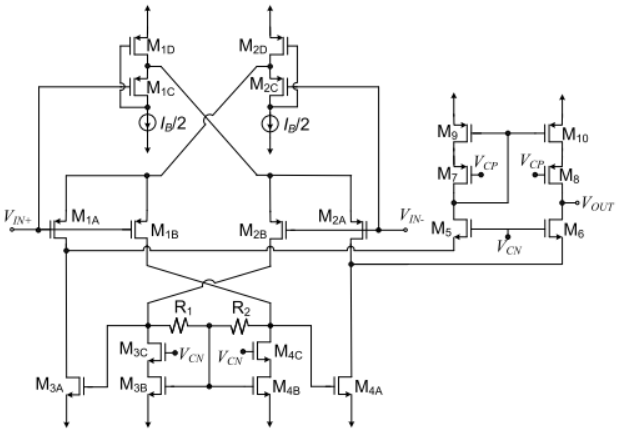

Fig. 1. *Super Class AB-Recycling Folded Cascode* OTA

A. Input Differential Pair (PMOS)

In biomedical signal acquisition systems, the input transistors play a crucial role in determining both the noise performance and the overall transconductance efficiency of the OTA (Lee, 2014). This makes their design particularly significant, not only from a performance standpoint but also as a key learning element in analog circuit design courses. The input differential pair is implemented using PMOS devices to minimize 1/f (flicker) noise, which is dominant in the low-frequency range of physiological signals.

The total current budget is strictly constrained to meet the ultra-low power requirement of 337.5 nW. Accordingly, a portion of this current is allocated to input stage, resulting in a sub-nanoampere quiescent drain current for each PMOS input transistor (M1, M2). To maximize transconductance efficiency under such ultra-low current conditions, the input pair is biased in the deep weak inversion region. This operating region is particularly important in both research and education, as it illustrates the trade-off between power consumption and device efficiency.

Using these parameters, the required aspect ratio of the transistors is calculated as follows:

$$\left(\frac{W}{L}\right)_1 = \frac{I_{D1}}{(I_D/(W/L))} \approx 0.24$$

The channel length is held constant at a conservatively large length of L = 5 µm to suppress the Channel Length Modulation (CLM) and to achieve the maximum amount of intrinsic self-gain ($g_m r_o$). Scaling this length by the aspect ratio that has been calculated would give the final designed width:

$$W_1 = 0.24\ X\ 5\ \mu m = 1.2\ \mu m$$

B. Current Mirror and Cascodes (NMOS)

Accurate current replication in the NMOS current mirrors and folding cascode transistors (M3–M6) is critical to the overall performance of the RFC architecture. These devices significantly influence key parameters such as gain, CMRR, and output stability (Garde, 2018). From an educational standpoint, their design provides an important case study in understanding trade-offs between device efficiency, output resistance, and voltage headroom in analog circuits.

Unlike the input differential pair, which is primarily optimized for transconductance efficiency, the NMOS current mirrors and cascode devices must balance multiple design constraints, including output resistance (r_o), voltage headroom, and device mismatch. To achieve this balance, these transistors are biased in the moderate inversion region, which offers a practical compromise between efficiency and linearity while ensuring sufficient voltage headroom to achieve the targeted high CMRR of 136.36 dB.

Using these parameters, the required aspect ratio of the transistors is calculated as follows:

$$\left(\frac{W}{L}\right)_3 = \frac{I_{D3}}{(I\_D/(W/L))} \approx 1.03$$

In order to dampen threshold voltage change (ΔVTH) which compromises CMRR, the model by Pelgrom requires the active device area (W L) to be as large as possible (Pelgrom, 2003). Moreover, the channel length is left large in value, L = 5 u m to obtain the desired value of the output resistance to obtain the required 75.73 dB DC gain. Division of this length by the calculated aspect ratio will give the width that is needed:

$$W_3 = 1.03 \times 5\ \mu m = 5.15\ \mu m$$

This makes sure that the recycling and cascode transistors give the required accuracy of current mirroring and output impedance.

C. Active Pseudo-Resistor Load (NMOS)

To achieve the desired high DC gain without using the excess silicon area needed by passive mega-ohm resistors NMOS-based pseudo-resistors are used as active loads. Linear resistor These devices are biased to operate in the linear (triode) region where their equivalent on-resistance (R_{on}) is:

$$R_{on} = \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_{TH})}$$

To achieve the 75.73 dB open-loop gain, the required equivalent load resistance must be in the tens of mega-ohms. To maximize $R_{on}$for a fixed bias voltage (V_{GS}), the aspect ratio (W/L)should be minimized as much as practically possible. However, in deep submicron technologies, very small device dimensions can introduce short-channel and narrow-width effects, requiring careful design consideration. Therefore, the width of the pseudo-NMOS devices is chosen near the practical minimum for matched analog design in this process, i.e., $= 120\ nm$. This step also highlights an important design trade-off, which is useful for understanding device optimization in analog circuit design. Rearranging the resistance equation to determine the required channel length for achieving the target mega-ohm resistance results in a significantly large channel length requirement:

$$L_{pseudo} = R_{on} \cdot \mu_n C_{ox} \cdot W \cdot (V_{GS} - V_{TH})$$

Depending on the gain target and output conductance required to achieve the target, the length will be computed and adjusted to the value of L = 8.64 µm. This ratio of extreme aspect (W/L ≈0.0138) is to guarantee the maximum incremental resistance to guarantee the high gain, and save large layout space as opposed to the conventional passive elements, without requiring further static power consumption of its own [20, 30].

III. Proposed Architecture

The suggested OTA design employs the energy-optimized Super Class-AB Recycling Folded Cascode topology explored in first (Garde, 2018). This circuit meets the demanding specifications of biomedical signal amplification:very low quiescent power, high open-loop gain and able to drive large capacitive sensor loads efficiently.

In addition to its circuit-level benefits, the architecture is embedded as a sophisticated example problem in the proposed learning framework and allows students to experiment with fundamental low-power design principles such as current reuse, dynamic biasing, and transconductance improvement. This analysis allows students to explore how changing architectural choices affects performance metrics based on simulation, and ultimately formulates their understanding of the trade-offs between power efficiency, gain, and transient response.

Accordingly, the proposed OTA is unique in two ways: it provides a high-performance solution for biomedical AFE applications and dual role of an educational tool for teaching state-of-the-art analog design skills in both research and classroom settings.

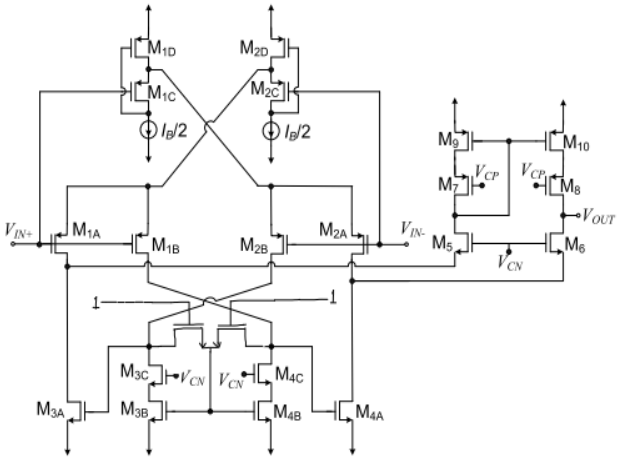

Fig. 2. *Schematic of the proposed RFC OTA for bio-medical applications*

A. Class-AB Dynamic Boosting

The Class-A OTAs used in contemporary designs are extremely limited in slew-rate, due to the constraints imposed on the remaining circuit outputs by the fixed bias applied. To reduce this critical drawback, the new design uses an adaptive biasing circuit on the input differential pair (Garde, 2018). This adaptive biasing is provided by means of Flipped Voltage Followers (FVFs) cross-coupled to input transistors. The FVFs have a closely regulated and ultra-low static current of 337.5nW under quiescent conditions. As a large differential input signal is however applied, the FVFs permit a large increase in the dynamic currents much above the quiescent bias limit, as if the available transconductance and charging current were multiplied on command.

B. LCMFB and Pseudo-NMOS Active Load Novelty.

In addition to adaptive input biasing, the architecture also employs a LCMFB network at the folding nodes of the recycling mirrors to further enhance dynamic current boosting and the gain-bandwidth product (GBW). In conventional Super Class-AB implementations, the LCMFB network relies on passive polysilicon resistors to generate the required voltage drops (Garde, 2018). However, this becomes a significant limitation in miniaturized biomedical applications. Achieving the required 75.73 dB DC gain for precise bio-signal acquisition demands resistance values in the mega-ohm range. Implementing such large passive resistors in 45 nm CMOS technology results in excessive silicon area, making it unsuitable for high-density implantable systems.

To address this issue, the proposed architecture replaces these area-intensive passive resistors with active pseudo-NMOS loads. These devices are carefully sized (as described in Section 2.3) with $W = 120\,nm$and $= 8.64\,\mu m$, and are biased in the linear (triode) region. This allows them to realize the required high equivalent resistance (R_{on}), ensuring the desired DC gain and a CMRR of 136.36 dB. This modification also provides a practical example of area-efficient design techniques in modern analog circuits.

With this architectural change, the design retains the dynamic Class-AB boosting capability and high power efficiency of the base topology, while significantly reducing layout area, making it well-suited for 45 nm biomedical analog front-ends.

IV. Simulation Results And Discussion

The simulation of the proposed ultra-low-power Class-AB Recycling Folded Cascode OTA was done on the 45 nm Generic Process Design Kit (GPDK) in Cadence Virtuoso. In order to capture an accurate model of the target environment of a wearable biomedical sensor interface, the supply voltage was adjusted to 1 V and a 20 pF load capacitor (CL) was placed across the output (Sansen, 2012).

A. AC Response

To analyze the small- signal performance and stability of the amplifier, an AC analysis was conducted. The proposed OTA has a high DC open-loop gain of 75.73 dB as shown in Fig. 3. The source of this high gain is mainly due to the huge increment of resistance that is offered by the new pseudo-NMOS active loads that work in the deep triode region. The unity-gain bandwidth and the phase margin are the key parameters when it comes to closed-loop stability. The proposed design has a very good phase margin of 84.02°. This stability ensures a strong response without excessive ringing even with large capacitance of capacitive loads of high density typically found in high-density arrays of electrodes.
Fig.3 shows the phase response of the OTA as a function of frequency. At low frequencies, the phase starts close to 0° and gradually decreases as the frequency increases due to the presence of multiple poles in the circuit. The phase continues to drop at higher frequencies, indicating the dynamic behavior of the amplifier and confirming stable operation with an adequate phase margin.

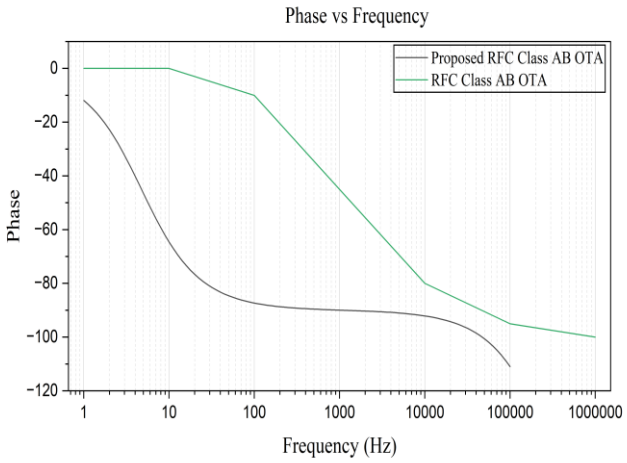

Fig 3. Phase vs frequency plot

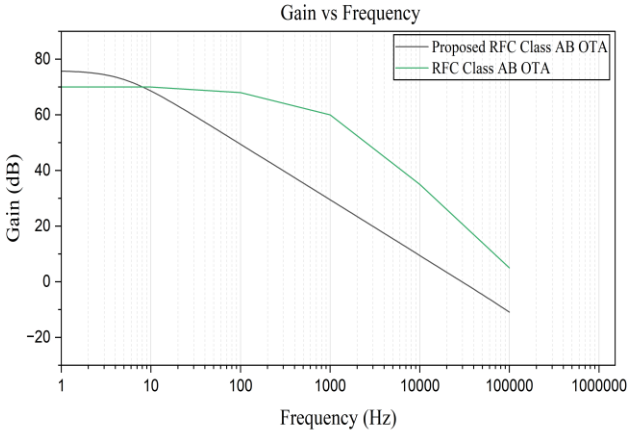

Fig 4. Magnitude vs frequency plot

Fig.4 illustrates the magnitude (gain) response versus frequency. The plot shows a high DC gain at low frequencies, which gradually decreases with increasing frequency due to the effect of dominant and higher-order poles. The slope of the curve indicates the bandwidth limitation of the OTA and

demonstrates the frequency-dependent gain roll-off typical of operational transconductance amplifiers.

B. Transient Response and Power Consumption

Transient response was conducted to confirm the efficiency of Class-AB dynamic boosting mechanism. Fig.5 demonstrates how the OTA responds to a huge input step. The adaptive biasing network is able to achieve large dynamic charging currents to the load on demand despite having a highly constrained, ultra-low quiescent power of only 337.5 nW of operation. In such a way, the OTA has a positive slew rate of 0.024 V/ μs throughout the load of 20 pF. This effectively breaks the basic speed-power trade-off that would be inherent to the standard Class-A architectures that would be effectively throttled by their sub-nanoampere tail currents (Garde, 2018), (Razavi, 2020).

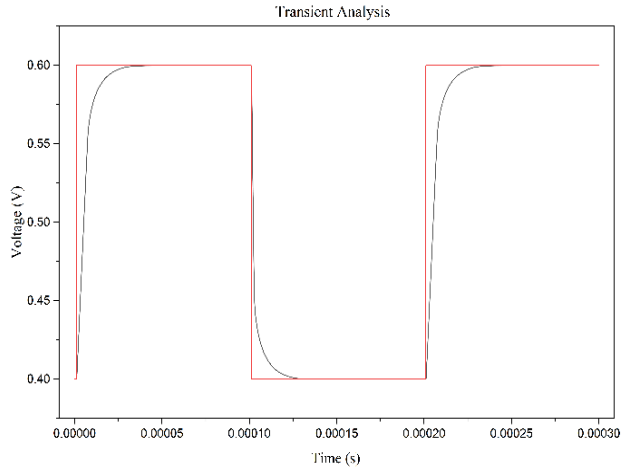

Fig.5 transient Analysis plot

C. Common mode Rejection Ratio

D. In biomedical uses (e.g. EEG recording or ECG recording) physiological signals can be seriously distorted by large-scale common-mode interference, in particular, powerline noise at 50/60 Hz (Kasipogula, 2024). Thus, the CMRR of the analog front-end needs to be extremely high. The proposed OTA has an excellent DC CMRR of 136.36 dB as indicated in Fig. 5. This is because of the high rejection due to the accurate sizing methodology of the gm/ID current mirrors used to achieve the NMOS current mirrors which reduces the mismatch of threshold voltages as well as the high output impedance of the pseudo-NMOS loads

E. Performance Comparison

To highlight the advantages of the proposed architecture, its performance is compared with the base Super Class-AB topology and other recent state-of-the-art OTAs in Table II. The most significant achievement of the proposed design is the drastic reduction in power consumption while maintaining high precision. Compared to the base Super Class-AB architecture presented in, which consumes 100 µW, the proposed 45 nm design operates at just 337.5 nW a power reduction of nearly 300 times (Wu, 2025). Furthermore, the integration of pseudo-NMOS loads (Galan, 2007), (Hastings, 2006) eliminates the need for the massive passive polysilicon resistors utilized in, significantly improving area efficiency for deep sub-micron integration. Despite the nano-watt power budget, the proposed OTA maintains a highly competitive gain 75.73 dB and exceptional CMRR 136.36 dB, proving its high suitability for next-generation implantable bio-sensors (Kasipogula, 2024).

Table 1 presents a comparative analysis of the proposed OTA with previously reported designs in references (Chen, 2024), (Kasipogula, 2024), (Garde, 2018), and our work. The earlier designs in and were implemented using 180 nm CMOS technology, while the base paper used 500 nm technology. In contrast, the proposed OTA is implemented in 45 nm CMOS technology, enabling improved device scaling and power efficiency (Ardalan, 2003). The proposed design operates at a 1 V supply voltage, which is lower than the 1.8 V used in (Kasipogula, 2024) and equal to the supply used in (Chen, 2024) and the base paper (Garde, 2018). The load capacitance considered for the proposed OTA is 20 pF, which lies between the values used in the compared works.

TABLE I
PERFORMANCE COMPARISON WITH STATE-OF-THE-ART OTAS

Parameter	(Kasipogula, 2024)	(Chen, 2024)	(Garde, 2018) Quoted for comparison	Proposed OTA (Simulated)
Technology (nm)	180	180	500	45
Supply Voltage (V)	1.8	1.0	1V	1.0
Load Capacitance (pF)	15	10	70	20
DC Gain (dB)	65.2	72.0	76.8	75.73
Phase Margin (°)	62	55	75.1	84.02
CMRR (dB)	85	90	112	136.36
Power Consumption	1.2μW	2.5 μW	100 μW	337.5 nW

In terms of performance, the proposed OTA achieves a DC gain of 75.73 dB, which is comparable to the base paper (76.8 dB) and higher than the gain reported in (Kasipogula, 2024). The phase margin of 84.02° is the highest among all compared designs, indicating improved stability.

Additionally, the proposed OTA features a CMRR of 136.36 dB and an ultra-low power consumption of 337.5 nW exceeding similar designs published in previous works. Although these results effectively confirm the capability of the presented architecture from a circuit point-of-view, their primary importance in this work is as quantifiable learning outcomes within our simulation-driven framework.

Examining these performance metrics allows the learner to directly correlate design decisions—like biasing techniques, current reuse and device sizing—with enhancements in critical parameters such as common-mode rejection, stability and power efficiency. How this quantifiable assessment allows students to go from theory to evidence-based design intuition.

In addition, high performance under tight power and area constraints creates a realistic setting to investigate practical design tradeoffs. The ON resistance of a BJT can be approximated as a resistor under the conditions where it is

activated above certain bias voltage, meaning that the proposed OTA is not only technically feasible, but also an excellent teaching tool to support students in strengthening general circuit design concepts regarding low-power analog circuits.

CONCLUSION

In this work, the authors propose a data-driven-based experiential learning framework to simulate the design and optimization of a Class-AB recycling folded cascode (RFC) OTA for biomedical analog front-end applications based on 45nm CMOS technology. Under this framework, the design process is a sequence of iterative simulation → performance evaluation → parameter refinement tasks, allowing learners to simultaneously optimize circuit performance as well as learn more about analog design principles.

An instructional design module is proposed that adopts a dynamic Class-AB boosting mechanism to alleviate the speed–power trade-offs of conventional Class-A topologies. With the help of guided simulations, learners explore how adaptive biasing can increase instantaneous current handling capability during dynamic operation to enhance slew rate and overall dynamic performance without an associated static power penalty. Students can see the link between biasing strategies and large-signal behavior.

The other main aspect of the framework is to substitute traditional passive polysilicon resistors in the LCMFB with small pseudo-NMOS active loads. These loads can be drawn in the deep linear region to have very high incremental resistance and save on silicon area. This change is included as a comparative design task, allowing students to assess trade-offs in area efficiency, linearity and gain, and the design realities of active vs passive implementations.

In addition, the framework as a fundamental learning material utilizes g_m/I_D based design concept that directs learners to conduct an examination of device working in subthreshold region. Students gain intuition about transconductance efficiency, power consumption, and circuit behavior by iteratively tuning device parameters and observing quantitative trends that form between them.

Results of the simulation performed using this framework show that the presented OTA provides a DC open-loop gain of 75.73dB, CMRR up to 136.36 dB and a phase margin of 84.02° when driving a 20pF capacitive load. The circuit operates at a quiescent power of 337.5 nW at a 1 V supply and a positive slew rate (+SR) of 0.024 V/µs; these results serve as performance baselines within the learning framework that helps learners verify design choices and connect architectural features with tangible metrics.

Given its ultra-low power consumption, excellent common-mode rejection, and smaller silicon area, the proposed pseudo-NMOS Class-AB RFC OTA is ideally suited for next-generation availability in wearable and implantable biomedical sensor systems. More importantly, the work presented here lays down an entire educational framework in which simulation-based experiential learning aids the understanding of some advanced techniques for analog design such as current recycling, dynamic-biasing, implementation of active loads, and operation deep into subthreshold region in modern CMOS technologies.

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