

MAPLE Model: A Blended ARCS-PSIS Approach to Enhance Gen-Z Engagement in Core Engineering Courses

¹Kendaganna Swamy S, ²Hemanthakumar R Kappali, ³Manjunath G, ⁴Shilpa K R, ⁵Sadyojatha K M, ⁶Rajasree M

^{1,6}Assistant Professor, Department of Electronics & Instrumentation Engineering, RVCE, Bengaluru

^{2,3,4}Assistant Professor, Department of Electronics & Communication Engineering, BITM, Ballari

⁵Professor & Head, Department of Electronics & Communication Engineering, BITM, Ballari

¹ kendagannaswamys@rvce.edu.in

²hemanthakumar@bitm.edu.in

³manjunathg@bitm.edu.in

⁴shilpa@bitm.edu.in

⁵sadyojatha@bitm.edu.in

⁶rajasreepm@rvce.edu.in

Abstract—Gen-Z students often struggle with concentration and engagement in traditional classroom settings, particularly in core engineering courses like Very Large-Scale Integration (VLSI) Design, which are both concept-heavy and abstract. These learners, being digital natives, prefer interactive, collaborative, and application-oriented learning environments. Traditional lecture methods often fail to sustain their attention or motivation. To overcome this challenge, this paper introduces the Motivation-Aligned Peer Learning Environment (MAPLE) Model, a blended pedagogical framework that combines the Attention, Relevance, Confidence, Satisfaction (ARCS) motivational model with Peer-Supported Independent Study (PSIS). The ARCS component enhances theoretical learning by capturing attention, building relevance, and fostering confidence and satisfaction through structured and interactive delivery methods. Meanwhile, the PSIS component empowers students to explore practical applications through peer collaboration, hands-on activities, and independent learning in lab environments. This paper presents the design and implementation of the MAPLE Model in a third-year VLSI Design course and evaluates its effectiveness through quantitative and qualitative analyses. The results demonstrated significant improvements in academic performance, peer collaboration, and overall course satisfaction. This study concludes that the MAPLE Model is a scalable and effective instructional strategy for improving engagement and outcomes in core engineering education for Gen-Z learners.

Keywords—ARCS Motivational Model; CADENCE Tool; Gen-Z; MAPLE; Peer-learning; VLSI.

ICTIEE Track: Innovative Pedagogies and Active Learning

ICTIEE Sub-Track: Collaborative and Experiential Learning Models

I. INTRODUCTION

CORE engineering courses, especially those rooted in abstract concepts like VLSI Design, pose a unique

challenge to undergraduate learners. VLSI requires a deep understanding of both theory (such as CMOS fabrication principles, circuit analysis, timing constraints) and hands-on skills (such as schematic design, layout, and simulation using tools like CADENCE or XILINX). Despite its relevance in the semiconductor and electronics industry, VLSI is often regarded by students as complex and disconnected from real-world applications. This perception, coupled with the demanding technical depth of the course, often results in disengagement, low academic performance, and reduced interest in pursuing further studies or careers in the field (Dawn, 2013).

The Gen-Z learners, who are digital natives accustomed to fast-paced, interactive, and highly visual content. Traditional lecture-based teaching, static slides, and rigid lab sessions no longer resonate with their learning preferences. Research has shown that Gen-Z students prefer learning environments that are engaging, personalized, collaborative, and outcome-driven (Felder & Brent, 2009; Gamson, 1991; Prensky, 2001). In this context, there is an urgent need to reimaging pedagogical approaches that can hold their attention, foster deep understanding, and create intrinsic motivation. The goal is not merely to teach content, but to inspire curiosity, build confidence, and cultivate critical thinking and also to cater the manpower for the country to build strong human resource to VLSI industry (Hora & Ferrare, 2013; Richardson & Swan, 2003). As per the report from the NASSCOM, VLSI core sector likely seeing increased hiring due to the growth of semiconductor design and fabrication. India has a significant presence in global chip design, with 120,000 engineers currently, and plans to expand that to 1.2 million by 2032.

To address these challenges, we propose the MAPLE Model—a blended pedagogical framework that combines the

Hemanthakumar R Kappali

Department of Electronics & Communication Engineering, BITM, Ballari
hemanthakumar@bitm.edu.in

ARCS model of motivational instruction with the PSIS learning strategy. The ARCS model serves to capture and maintain student motivation throughout the theoretical portions of the course (Keller, 1987). By delivering the talks on the concept and theory the attention of the student on VLSI course is grabbed. The relevance of the course content is connected to the applications and career, deservetime and effort. Confidence is boosted through introducing demonstration and procedural experiments using industry standard tools like CADENCE. The confidence building in the students is made using simulation and verification of design-based tasks as mentioned in Fig 1.

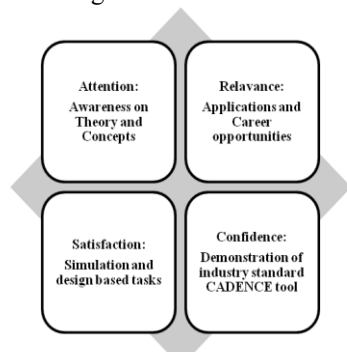


Fig. 1. ARCS Model for VLSI Design

In parallel, the PSIS framework supports students to acquire skill set through laboratory and project environments by promoting collaborative independent learning in peer groups (Topping, 2005; Webb, 1989). Fig 2 shows the PSIS framework which enhances VLSI learning by enabling students to work collaboratively on practical experiments and design-based problems. The peer groups develop and simulate CMOS logic gates using tools like CADENCE. By troubleshooting layout-versus-schematic (LVS) errors through shared independent insights and engaged peer mentoring. The proposed model builds the conceptual clarity with improved hands-on experience by applying critical thinking on designing a 1-bit Static Random Access Memory (SRAM) using industry level CADENCE tool.

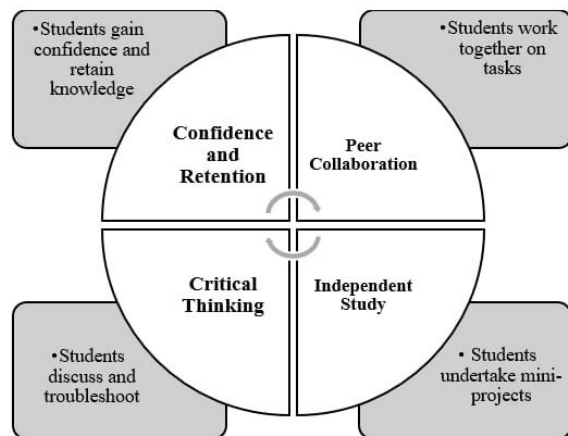


Fig. 2. PSIS Framework Learning Cycle

As a case study, the MAPLE Model was implemented in the VLSI Design course offered in the fifth semester of the Electronics and Communication Engineering undergraduate

program. The course delivery was restructured into three learning phases (i) ARCS-based theoretical engagement, where interactive lectures and digital tools were used to ensure topic-level motivation (ii) peer-supported lab sessions, where students worked in guided teams to simulate and analyze circuits in dependently and (iii) reflection and feedback, involving self-assessment and peer review mechanisms. This case study not only tested the effectiveness of the MAPLE Model in a real classroom setting but also evaluated the impact of this approach through quantitative analysis of exam scores and qualitative feedback from students. The results provide compelling evidence of improved engagement, deeper learning, and greater satisfaction among Gen-Z learners in a core technical course.

II. RELATED WORK

Motivation and engagement have been recognized as critical factors for effective learning, especially in core engineering courses. The ARCS model (Keller, 1987) implemented in many technical disciplines, to improve the learner attention and satisfaction, while (Kaveri et al., 2016) applies the model in STEM classrooms to increase performance and reduce dropout rates.

Innovative approaches are essential to enhance engineering education, particularly in VLSI courses. Several studies emphasize the importance of hands-on learning and integrating industry-relevant tools to bridge the gap between academia and industry demands (Madhavi et al., 2024; Prasad & Goel, 1993).

Peer-supported and collaborative learning frameworks also show promising results. The PSIS method has proven effective in fostering deeper conceptual understanding and self-directed learning, particularly when integrated with project-based lab activities (Huang, 2019; Sandoval-Lucero et al. 2012). In electronics engineering, (Ferro et al., 2025) emphasizes the value of team-based learning in enhancing circuit design skills and promoting active learning environments.

Further, several studies have explored Gen-Z students' learning preferences. According to (Meeghapola & Thilakarathne, 2019), digital-native learners respond better to blended, interactive, and collaborative pedagogies than traditional lecture-based models. These findings provide strong justification for integrating ARCS and PSIS strategies—leading to the development of the MAPLE Model as a unified pedagogical solution.

III. METHODOLOGY

The proposed MAPLE Model was implemented with a set of 60 students in the fifth semester of the Electronics and Communication Engineering (ECE) program. These students were part of one of the two existing sections, totaling 127 students. The selected section was chosen to pilot the MAPLE framework in the context of a core course: VLSI Design. As illustrated in Fig 3, the MAPLE Model operates through two concurrent learning pathways—the Theory Path, structured around the ARCS motivational model, and the Practice Path, built upon the Peer-Supported Independent Study (PSIS) framework. This dual-path structure was designed to ensure that

students engage meaningfully with theoretical concepts while simultaneously developing practical design skills in a collaborative, peer-driven environment.

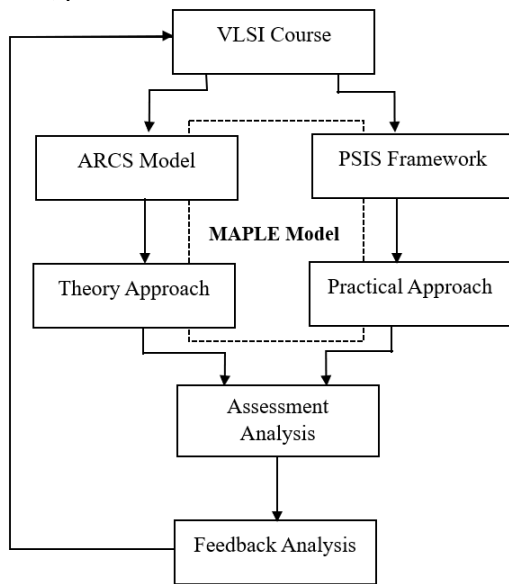


Fig. 3. Proposed MAPLE Model

To demonstrate the model's effectiveness, the design of SRAM was selected as a representative case study. The implementation unfolded across three instructional stages. In the first stage, during a one-hour theory session, the instructor applied the ARCS model. Attention was captured by linking SRAM design to its real-world application in processor caches. Relevance was established by emphasizing the importance of memory design in digital systems. Confidence was nurtured through a step-by-step explanation of 1-bit SRAM cell design at the transistor level. This systematic approach helped build a solid conceptual foundation for students.

In the second stage, a three-hour lab session was conducted before moving to the satisfaction element of the ARCS model. Here, students engaged with the PSIS framework. Working in small groups, they designed and simulated a 1-bit SRAM using the CADENCE tool. The peer-supported structure of PSIS allowed students to mentor and assist one another, encouraging both tool familiarity and deeper understanding. This collaborative environment enhanced their conceptual clarity and promoted self-directed learning.

The third stage integrated theory and practice to further solidify student understanding. In the following theory session, the instructor introduced an application-level challenge by asking students to extend their 1-bit SRAM design into an 8-bit memory array suitable for processor platforms, thereby fulfilling the satisfaction element of the ARCS model. The associated lab sessions were then used for collaborative development of the full 8-bit SRAM architecture, allowing students to apply their learning in a real-world design scenario. This hands-on experience contributed significantly to their sense of accomplishment and mastery.

The same iterative, integrated approach was extended to other VLSI topics, such as Arithmetic Logic Unit (ALU) Design—where students moved from understanding logical units in theory to implementing them at the gate level in practice. The Analog Amplifier Design—where theoretical concepts like

gain and biasing were followed by circuit simulation using SPICE; and Three-Stage Pipeline Design—where instruction flow was taught in class and then implemented as a pipelined data path in the lab. Weekly contact hours were consistently distributed as three hours for theory sessions and three hours for lab sessions.

Overall, this synchronized methodology fostered both cognitive understanding and practical skills development. The blending of ARCS and PSIS ensured that the MAPLE Model addressed the motivational and collaborative needs of Gen-Z learners, who benefit most from interactive and engaging educational environments.

During the initial phase of the activity, learners faced difficulty adapting to this new learning approach as it was different from traditional classroom methods. It was difficult to manage group dynamics and balance participation when working with classmates of varying skill levels. Also, teachers experienced a significant challenge in coordinating regular lab slots, implementing this new pedagogy, and managing ongoing classroom activities. Periodically feedback has been collected to correct and overcome the difficulties in implementing the model.

The following section presents an analysis of the model's impact using both quantitative measures, such as exam scores and assignment performance, and qualitative indicators, including student feedback and classroom engagement.

IV. RESULT AND ANALYSIS

This section presents a comprehensive evaluation of the MAPLE model's impact on student engagement and academic performance in the *VLSI Design* course. The findings are discussed under two dimensions: quantitative analysis, which examines measurable performance improvements, and qualitative analysis, which captures student perceptions, feedback, and experiential reflections. Together, these insights illustrate the extent to which MAPLE model enhances both cognitive understanding and peer-supported learning.

A. Quantitative Analysis

The MAPLE model, with its integrated hybrid learning pathways, enabled students to engage deeply with theoretical concepts while simultaneously strengthening practical design skills in a collaborative, peer-supported setting. To evaluate its effectiveness against the conventional lecture-based approach, a set of 60 students was assessed through Continuous Internal Evaluation (CIE) and Semester End Examination (SEE) scores.

The CIE comprised assignments, quizzes, and class tests for both theory and practical components of the VLSI Design course, while the SEE provided a comprehensive evaluation of the entire syllabus.

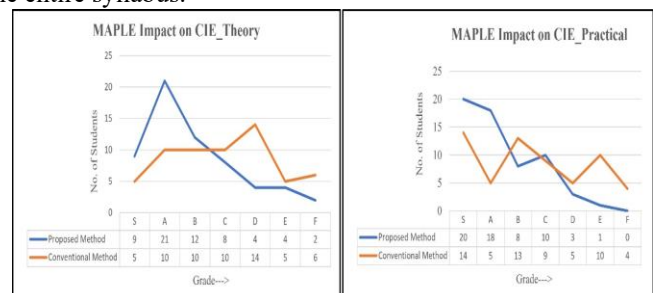


Fig. 4. MAPLE model impact on CIE Performance

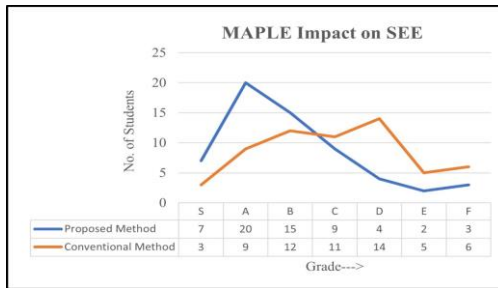


Fig. 5. MAPLE model impact on SEE Performance

Fig 4 and 5 illustrate the shift in grade distributions for CIE and SEE, respectively. Performance categories included S (Outstanding), A (Excellent), B (Very Good), C (Good), D (Above Average), E (Average), and F (Fail). Results indicate a clear upward shift in academic performance with MAPLE model implementation, with a marked reduction in lower grades (D, E, F) and an increase in higher grades (S, A, B). Notably, students who performed well in CIE also maintained comparable success in SEE, indicating consistent knowledge retention and application.

A key trend emerged in the CIE component analysis—average scores in practical lab assessments consistently outperformed those in theory-based evaluations. This suggests that MAPLE model emphasis on experiential, hands-on engagement fostered stronger conceptual clarity and skill application, particularly in design-oriented tasks.

During the MAPLE activity, formative evaluations were carried out to track participants' progress in technical comprehension, group interaction, and individual preparedness. Based on the comprehensive evaluation of prelab quizzes, peer assessments, and self-reflection ratings, the high-performing students have been identified. Further, they are encouraged to undertake task-based industry training on advanced VLSI design. A benchmark of 85% is set to identify high performers. 15 out of 60 (25%) students scored more than 85%. After the implementation of group-based PSIS learning, Students demonstrated a substantial enhancement from an average pre-test score of 75.9% to a post-test score of 80.61%, with a good correlation ($r = 0.84$) reflecting robust consistency in learning and this improvement is statistically significant, as evidenced by the p-value of less than 0.01. The standard deviation decreased from 8.88 (individual scores) to 2.85 (group averages), suggesting that learning through MAPLE model promoted more consistent learning outcomes across students through collaborative learning and reduced performance disparities.

B. Qualitative Analysis

The qualitative evaluation incorporated student reflections, feedback on learning experiences, and perceptions of faculty support. Using an eight-question survey on a five-point Likert scale, responses captured in Fig 6 demonstrate strong positive sentiment towards the MAPLE framework.

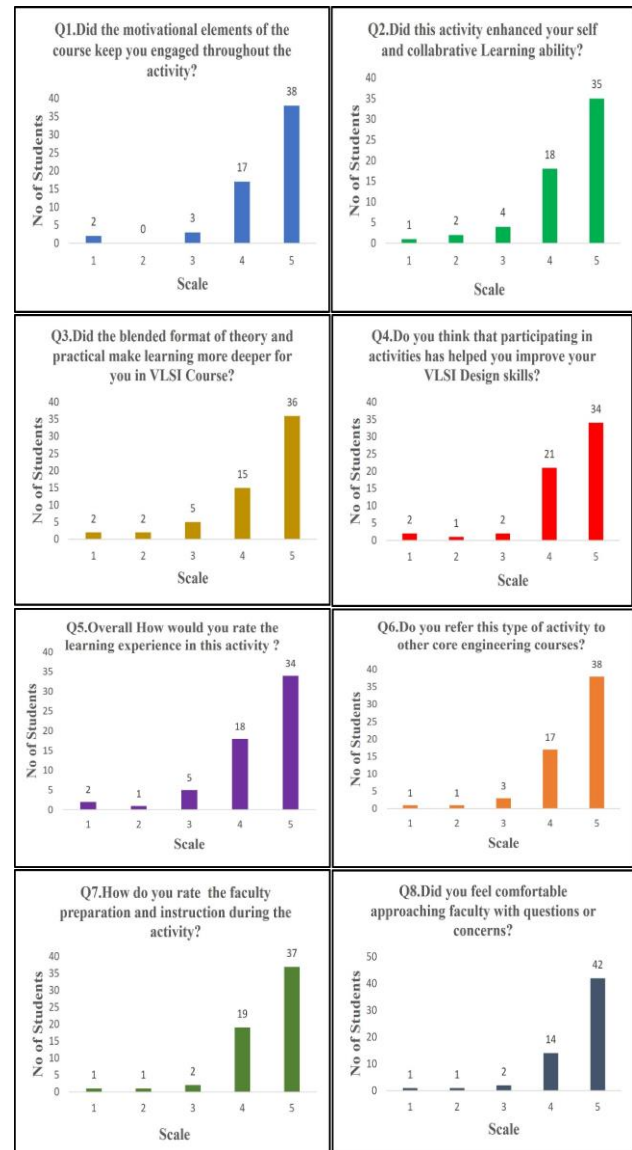


Fig. 6. MAPLE model implementation-reflections and feedback

More than 85% of students (Q1 and Q3) valued the blended format that integrated theoretical and practical learning, especially when linked to motivational, real-world VLSI applications. Effective peer collaboration was also highlighted, with 53 out of 60 students rating teamwork and mutual support as *highly satisfactory* (Q2). Importantly, 90% of respondents (Q6) expressed a desire to see MAPLE-based activities implemented in other core engineering courses.

Students attributed improved retention and application of concepts to well-structured faculty guidance and activity design. They also reported feeling comfortable in seeking clarifications during both structured and informal Q&A sessions (Q7 and Q8), indicating that the model fostered an approachable and supportive learning environment.

Based on the analysis, both quantitative performance gains and qualitative feedback confirm that the MAPLE model significantly enhances student engagement, knowledge retention, and collaborative skills. Its focus on blending theory with hands-on practice, supported by continuous feedback,

positions it as an effective pedagogical approach for complex, design-intensive engineering courses such as *VLSI Design*.

CONCLUSION

The integration of the ARCS motivational model with the PSIS framework in the proposed MAPLE Model provided a robust blended learning environment for Gen-Z engineering students. By aligning motivational strategies with collaborative and hands-on learning, the model successfully bridged the gap between theoretical concepts and practical application in VLSI design. Numerical evidence confirms that the MAPLE approach led to 8–10% higher academic performance, 23% higher practical success rates, and a 37% improvement in tool proficiency compared to traditional methods. Moreover, the qualitative benefits of increased engagement, peer interaction, and learner autonomy position the MAPLE Model as a sustainable pedagogical approach for core engineering courses. Future work will focus on extending this model to interdisciplinary domains such as embedded systems, IoT hardware design, and analog circuit design, while employing longitudinal tracking to assess its impact on employability and higher-order problem-solving skills. Furthermore, scaling the model across multiple institutions will help validate its adaptability to diverse learning contexts.

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