Implementing a 50:50 Theory and Lab Pedagogical Model for Verilog HDL: An Outcome-Based Approach

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***Abstract*—The 50:50 Theory-Lab Teaching Model is a successful model for providing Verilog hardware description language (HDL) course material to undergraduate engineering students, with a balanced approach to delivery through both theory (classroom) and lab (practical) experience. The model allows equal opportunities for students to gain both knowledge (theoretical) and hands-on experience (practical). The educational approach used by this model was tested with a group of sixty (60) undergraduate engineering students. The educational techniques associated with this model used the same tools used in the industry (ModelSim, Xilinx ISE, and Vivado), which were evaluated using a rubric that was later expressed as quantitative data. Statistical methods performed on this quantitative data revealed that the students in the 50:50 Theory-Lab Teaching Model performed more accurately when simulating their designs, were more efficient when debugging their designs, and had a greater understanding of the concepts related to the implementation of Verilog HDL compared to students taught through traditional lecture methods ($p < 0.05$) with large effect sizes (Cohen's $d > 0.80$). Therefore, the educational approach developed in this project is a cost-effective and flexible way of delivering course content, thereby enabling students to develop technical competencies and analytical skills and demonstrate job readiness, which meets the objectives of the OBE Principles and NEP 2020 Guidelines. Compared to the baseline, the inputs to this model resulted in an increase of +22%, +24%, and +22% for simulation accuracy, debugging performance, and project evaluation scores, respectively (p-value < 0.01, Cohen's d > 0.90). Furthermore, SPI improvements, 18.4%, SES efficiencies of 27%, and 21 Concept Retention Gain (CRG) support these findings.**

Keywords—50:50 ; Theory–Lab teaching model; OBE; NEP 2020; Verilog HDL

ICTIEE* Track—*Innovative Pedagogies and Active Learning
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I. INTRODUCTION

DIGITAL design education relies heavily on Verilog HDL as a foundation course; however, most educators depend on a traditional teaching method that allocates 80% to 90 % of class time to providing theoretical lectures to create digital designs without providing sufficient hands-on experience for learners. This lack of practical experience leads to limited debugging techniques and lower levels of design fluency, and ultimately does not prepare the learner for a career as an engineer.

To fill this gap in education and improve the learning environment for students, we developed the 50/50 Theory Lab Teaching Model. With this model, all theoretical concepts are immediately reinforced using laboratories in all courses. Therefore, it is consistent with the principles of OBE and the NEP 2020 recommendations regarding experiential learning. In addition, it is like the processes of industry-based VLSI and FPGA workflows, therefore, providing students with an authentic experience of how digital designs are created within these industries. The author in the paper (Li et al., 2023; Kumar & Singh, 2024) explains that integrating simulation-based labs into the teaching cycle improves both retention and problem-solving ability. Although there is an absence of high-quality empirical research evidencing the benefits of a 50:50 Ratio Approach to teaching HDL, there are many active learning approaches available; however, these generally do not incorporate real-time feedback, have limited simulation integration, and do not employ a balance between theory and practice when teaching HDL. This article intends to demonstrate an established 50:50 ratio approach for teaching HDL through the use of online judges that provide feedback on submitted code and test results, thereby enhancing learning beyond traditional hardware verification methodologies (Zhang, 2023).

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A. Structure of the 50:50 Teaching Model

In this approach, each Verilog HDL session is structured to include 50% theory and 50% practical hands-on practice. For example, a session may start with teaching behavioral modeling concepts (such as always blocks or procedural assignments), followed by lab activities in Xilinx ISE or ModelSim to simulate a 4-bit adder or finite state machine. Weekly modules are mapped to design tasks, ensuring that for every theoretical concept learned, a corresponding Verilog code is written, simulated and functionally verified in the lab. Most existing HDL pedagogy relies heavily on theoretical delivery, with minimal practical reinforcement. Related works and gap analysis are represented by Table I.

TABLE. I
RELATED WORKS AND GAP ANALYSIS

Model	Key Features	Gap in HDL Context	50:50 Model Advantage
Traditional Lecture	Heavy theory focus, minimal lab	Poor retention, low debugging exposure	Immediate application ensures retention
Project-Based Learning	Long-term projects, deep exploration	Lacks weekly reinforcement	Ensures ongoing practice
Flipped Classroom	In-class application, preclass lectures	Dependent on student preparation	Guaranteed exposure in-class
Peer Instruction	Conceptual discussion	No tool-based practice	Combines discussion with simulation

The 50:50 Model attempts to overcome this educational gap by delivering both theoretical conceptual instruction and practical application in a properly integrated manner. Using this methodology, students will receive reinforcement of their Verilog concepts through the ability to immediately simulate and analyze time-domain signals. By providing both a conceptual view of the way a design works and how it operates at the gate level, students will have a full understanding of their project outcomes. Through the lab portion of the course, students will develop their skills in creating test benches, analyzing waveforms, and debugging, which is a necessary skill set for engineers designing projects. This study aimed to evaluate the impact of the 50:50 Theory-Lab Model on the performance and engagement of Verilog HDL students. The hypothesis states that a "balanced" approach to instruction will yield superior debugging, conceptual understanding, and ultimately superior project results. The successful execution of the proposed model requires the availability of licensed simulation tools and adequate laboratory facilities. In addition, providing equal amounts of content within the confines of a limited course length will continue to be challenging.

B. Research Objectives and Hypotheses

Objectives

1. To apply 50:50 Theory-Lab delivery of Verilog HDL
2. To evaluate its impact on:
   a) simulation accuracy
   b) debugging proficiency
   c) conceptual understanding

To make a comparative analysis between the learning results of the students and the past applied teaching strategies (Traditional and Flipped models).

Hypotheses

H1: Students who receive their education in a 50/50 Model have better accuracy using simulation methods than students in traditional educational models.
H2: The 50/50 Model provides greater support for students' ability to debug and instills a higher level of confidence in students.
H3: A positive relationship exists between students' lab performance and theory examination scores.

II. RELATED WORKS

The positive impact of active learning methods in the education of technology-related fields has been discussed in earlier research, which has focused primarily on computing education initiatives based on a tool-driven instructional model. Peer Instruction is another method that the author uses to help physics and engineering instructors improve student comprehension of the concepts covered in each course. The author's approach to developing the 50/50 Model is based on applying balanced experiential learning techniques while combining traditional and non-traditional techniques of teaching and learning. Many current models for Dual Language Education (DLE) do not provide students with the opportunity for continuous and immediate feedback regarding their learning, nor do they offer hands-on or experiential learning experiences that are essential for the success of the DLE model.

The 50/50 Dual Language Model is an innovative bilingual education model created to support the success of traditionally underrepresented students while simultaneously allowing for the equal use of both languages within the same period of instruction. This model also allows for the development of both languages based on the content area of instruction, as well as on the time spent in each language, thereby encouraging students to become proficient in both languages, while also supporting the development of culturally inclusive environments (Deyasi, 2019). This article explores the challenges facing bilingual dual-language education, with a particular focus on balancing the competing needs of various communities. The authors state that it is essential for school principals to be aware of and navigate the divergent experiences and attitudes of each group's parents toward bilingual dual language education, especially given the role of each modern-day community in fostering student identity versus providing monetary advantages to their students' educational future (Halle, 2014). While this paper discusses the implementation of activating linguistic and cultural diversity within the classroom environment, it does not specifically mention or explain how the 50%/50% Dual-Language Model enhances opportunities for diverse learners through bilingual education, nor does it delineate the implications of different bilingual education models for diverse learners (Piccardo, 2022).The Balanced 50/50 Method for

Bilingual Learning allows the separation of the two languages used with all student populations, such as ELL's, by allowing the student to learn Literacy in both Languages, divided equally between both Languages, through Content Areas & Time(Gómez, 2010).

The 50/50 dual-language program provides equal instruction in both English and Spanish to allow all learners a chance to become bilingual and biliterate. This type of instruction allows English language learners (ELLs) and native speakers to be integrated as they enhance their language skills through collaboration; however, it is also an area where support is needed regarding assessment and training for teachers(Acosta, 2019). This article discusses to teach people from different backgrounds, especially those who speak multiple languages. Although it does not specifically mention the 50% 50% Dual Language Model, it discusses to use inclusive methods to help students learn in multilingual environments (Bisai, 2020).

This report presents a new model for Dual Language Instruction through 2-1-L2. The 2-1-L2 Model is structurally designed to support all students in becoming bilingual content users and enhance their global learning experiences within multicultural classrooms. However, it does not include any discussion about the 50/50 Dual Language Instruction model (Przymus, 2016). Dual Language programs support academic achievement for English Language Learners. This study tests a dual-language framework that combines the 90/10 and 50/50 models (Billy, 2019).The author states the importance of Dual Language (DL) education in improving the academic performance of a diverse range of learners by supporting their cultural identities (Culturally Responsive Teaching). By supporting the development and validation of all students' cultural identities through DL Education and CRT, students are allowed to thrive academically in a safe and supportive environment and achieve academic success at a higher level than those in other programs(Garza, 2020) (Kapoor, 2014).

TABLE II
COMPARISON WITH 50:50 MODEL

Model	Key Features	Comparison to 50:50 Model
Project-Based Learning	Long-term, open-ended problem solving	Lacks synchronous weekly theory–application alignment
Flipped Classroom	Pre-class video learning, in-class application	Dependent on student preparation, 50:50 ensures exposure
Peer Instruction	Concept checks, guided reasoning	Improves conceptual clarity but lacks a simulation application

This article (Alanís, 2011) explores dual-language educational programs as they pertain to the academic and social development of bilingual students. In addition to analyzing the collaborative learning opportunities that contribute to enhancing both Bilingualism and Biliteracy, this paper identifies some critical issues and challenges facing detailed language programs today due to the heterogeneity of many classroom environments. This report provides evidence that Dual-Language Immersion is effective in creating bilinguals and providing them with cognitive benefits and a greater understanding of culture among students from a variety of backgrounds. DLI will improve the overall success of a classroom through partnerships with families and communities(Alisoy, 2025).All the above-mentioned models improve student engagement and retention through various methods; however, the 50:50 model stands out because it provides a unique combination of both theoretical instruction and practical application within one interaction or session. This allows instructors to provide a structured approach to teaching technical subjects such as Verilog HDL, which require students to understand syntax as well as be able to verify their work through simulation. The comparison table in Table II supports this approach.

A. Methodology

2.1 Research Context

This rmodel was carried out at the Vidyavardhaka College of Engineering, Mysuru, in the Department of Electronics and Communication Engineering, India. Intervention that was put in place was a 12-week Verilog HDL course, which involved theory and laboratory-based testing. The course will have four credits and will be included in the core digital system design curriculum, according to the Outcome-Based Education (OBE) and NEP 2020 requirements.

2.2 Research Design

The effectiveness of the 50:50 Theory Lab Teaching Model was assessed using a quasi-experimental single-group pre-test/post-test study. The model was used during the semester, and the performance of the students before and after the application was compared using assessment metrics and feedback.

2.3 Participants and Sampling

The study involved 60 second-year undergraduate engineering course learners who were taking the Verilog HDL course. As the course is compulsory, a full cohort sampling strategy was selected to overcome the presence of bias and ensure equal exposure to the intervention.

2.4 Intervention Structure

The instructional design was systematic with a 50:50 proportionality in every session, with 50 percent of the time devoted to theory explanation and the other 50 percent devoted to respective simulation and coding exercises. These tools were ModelSim, Xilinx ISE, and Vivado.

2.5 Mini Projects

1. Verilog-based mini projects were written by the students using advanced concepts and simulation flows. Examples include:1. Arithmetic Logic Unit (ALU)
2. Traffic Light Controller
3. Seven-Segment Display Driver.
4. Priority Encoder

2.6 Data Collection Instruments

TABLE III
INSTRUMENT AND ITS PURPOSE

Instrument	Purpose
Pre and Post Assessment Tests	Measure improvement in conceptual understanding

Simulation Performance Scores	Evaluate coding accuracy and error resolution
Rubric-based Lab Assessments	Evaluate implementation and debugging skills
Mini Project Evaluation Rubrics	Assess applied learning
Student Feedback Survey	Collect learner perception and confidence levels

2.7 AI-Based Feedback Clarification

AI-based feedback can be called the use of an automated Natural Language Processing (NLP) sentiment analyzer to assess open-ended student feedback. Responses were divided into strongly positive, positive, neutral, and negative, similar to the instruments employed in learning analytics in educational technology studies.

2.8 Data Analysis Procedures

Quantitative data (test scores, simulation performance, project evaluations) were analyzed using

1. Paired t-tests
2. Correlation analysis
3. Effect size (Cohen's d)

Qualitative feedback was analyzed using the AI sentiment model to identify patterns in learner experience and engagement.The 50:50 model was implemented with 60 undergraduate engineering students. Each session was split evenly between theory (lectures and discussions) and lab work (coding, simulation, and debugging). The tools used included ModelSim, Xilinx ISE, and Vivado. Weekly topics were aligned with the corresponding lab tasks to ensure immediate application, as shown in Fig.1.

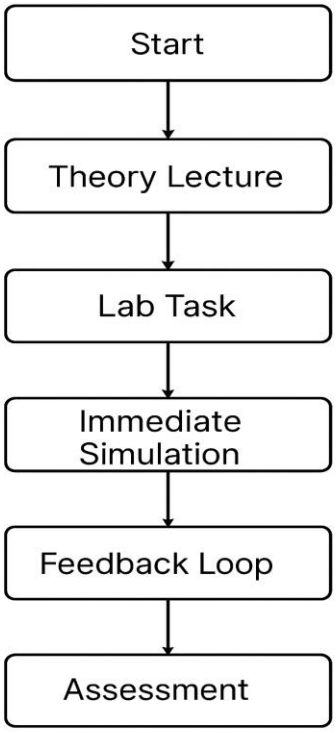

Fig.1. Methodology diagram

1) Data Collection

Student grades, laboratory evaluations, rubric scores, and AI-based feedback analysis were used for the evaluation.

2) Correlation Insights

Based on early indications, there appears to be a correlation between simulated laboratory performance and how well students understand theoretical concepts, as demonstrated through their viva and written examinations. Essentially, students who were more accurate in simulating laboratory work performed better theoretically than those who were not.

Implementation Framework

The pedagogical flow of the 50:50 model follows this cycle.

1. Theory Delivery
2. Lab Simulation of Concepts
3. Feedback and Debugging
4. Mini Project Application
5. Evaluation via Rubric

A 50:50 Theory/Lab Teaching Model was introduced to 60 undergraduate engineering students to support their learning of Verilog HDL. Each session consists of equal parts theory instruction through lectures and presentations first, followed by immediate application of what has been learned in a theory class to real-life situations through simulation and coding with software tools, such as ModelSim, Xilinx ISE, and Vivado. All laboratory exercises were designed to correspond with each week's theoretical topics so that students could connect all of their classroom learning to their laboratory work. Performance Data on this model includes all rubric score assessments for the courses evaluated, AI-generated feedback, and the accuracy of all simulations. These data were obtained to evaluate the outcomes of the 50/50 Teaching Model with respect to developing an understanding of theory, debugging ability, and practical capabilities. This methodology fosters a real-time feedback loop, allowing students to apply, simulate, and refine their understanding through hands-on engagement, aligning with the ((OBE) and NEP 2020 goals, as shown in Fig.2.

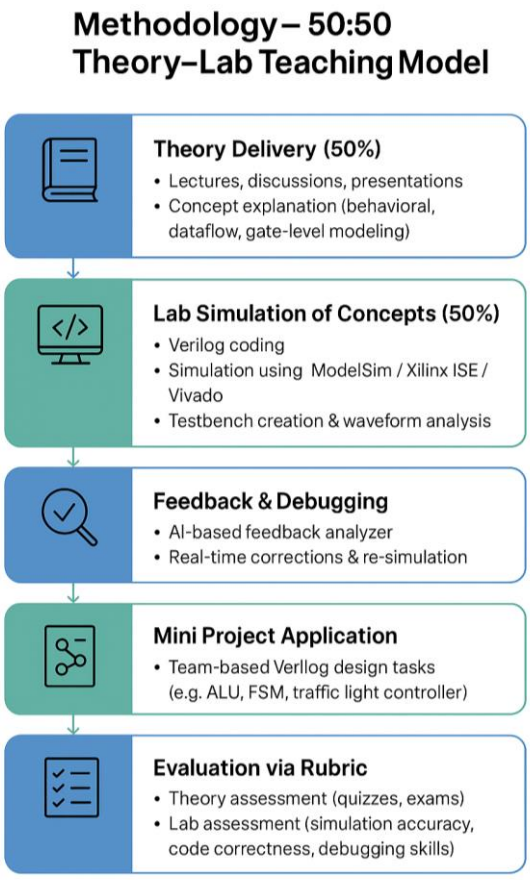

Fig.2. Methodology -50:50 Model

TABLE IV
50:50 THEORY AND LAB COMPONENT

Week/Session	Theory Component	Lab Component	Tools Used
1	Introduction to Verilog, syntax rules	Writing basic modules	ModelSim
2	Dataflow modeling	4-bit adder implementation	ModelSim
3	Behavioral modeling & procedural constructs	Simulation of sequential circuits	ModelSim
4	Testbench structure and simulation workflow	Writing and running testbenches	ModelSim
5	FSM design and modeling	Traffic light controller FSM simulation	Vivado
6	Hierarchical design	Modular ALU implementation	Vivado
7	RTL optimization and FPGA workflow	Timing analysis and waveform validation	Vivado
8–10	Mini project guidance and debugging	Project coding and presentation	Xilinx ISE/Vivado
11	Rubric-based evaluation	Debugging assessment	All tools
12	Post-test evaluation + Reflection	None	N/A

B. Student Outcomes and Skill Development

By employing the 50:50 model, students develop a robust understanding of the digital design flow from specifications to RTL coding and simulation. Theoretical learning provides students with a foundational understanding of gate-level models, data flow theory, and Sequential Logic. The lab portion reinforces a student's ability to read and write syntactically correct coding using Hands-on Practice.

Students will learn the following:

1. Create modular and hierarchical designs for HDL language Verilog.Their designs were simulated using simulation software and implemented using timing diagrams.
2. To find and remove logic and syntactical errors from their design using Visual Waveform-Analyzing software.
3. Work together with another student to complete a mini-project (i.e., ALU or Traffic Light Controller design).

III. RESULTS AND DISCUSSION

This section presents the findings of the present research, including the impact of the 50/50 Theory-Lab Model on participants' simulation accuracy, debugging ability, and comprehension of concepts, as well as comparisons with historical data gathered through the methods described in the methodology section. Table III compares the Traditional, Flipped, and Proposed 50:50 teaching models for Verilog HDL. Traditional lectures focus heavily on theory (90%) with minimal lab work and no simulation tools, leading to poor knowledge retention. In terms of balancing the use of tools and Peer Feedback in flipped classrooms, the proposed 60%/40% model produces mixed results due to the following factors: split equally between theory (50% of the Learning Experience) and labs (50%), and the Use of Comprehensive Simulation Tools such as Vivado and ModelSim. This Model uses AI Based feedback that enables real-time integration of learning improvement and corresponds with the ability to give each student Personalized Support for their Learning Process. The use of this form of model improves Conceptual Clarity, Practical Skill Development, and Overall Student Success. The verification of a 4-Bit Ripple Carry Adder was generated by simulating the Verilog Design with Model Sim. The output of the waveforms produced outputs identical to those expected; therefore, this demonstrates that the Carry Bits were successfully implemented through either propagation or Functional Simulation.

TABLE V
BENCHMARKING TABLE

Model	Theory (%)	Lab (%)	Simulation Tools	Feedback Method	Outcome
Traditional Lecture	90	10	None	Manual Feedback	Poor retention
Flipped Classroom	60	40	Partial	Peer-based	Mixed outcomes
Proposed 50:50 Model	50	50	Full (Vivado/ModelSim)	Al Feedback Analyzer	High concept clarity

The Theory Portion (50%) of the assessment evaluates Conceptual Knowledge, Syntax and Model Techniques, and Analysis of Design Flow for Conceptual Design methodologies. Assessment tools consist of written exams, short quizzes, and conceptual design-related assessment questions to measure students comprehend the analytical subject matter. The Lab Portion (50%) assesses a student's ability to code, design test benches, generate simulations, and validate outputs. The evaluative mechanisms used to evaluate students during their lab portion include Lab Records, Waveform Analysis, Screenshots and Lab Presentations of Mini-Projects. This rubric ensures a balanced evaluation of both theoretical knowledge and practical implementation skills (Table VI)

TABLE. VI
RUBRIC TABLE FOR VERILOG HDL - 50:50 THEORY-LAB MODEL

Component	Criteria	Weight (%)	Assessment Tools
Theory (50%)	Conceptual Understanding	15%	Written Exams, Viva Voce
	Syntax Accuracy (Always blocks, Modules, etc.)	10%	Written Code Samples, Short Quizzes
	Modeling Techniques (Dataflow, Behavioral)	15%	Problem-Based Questions, Design Justifications
	Design Analysis & Simulation Flow	10%	Written Assignments, Diagram Interpretation
Lab (50%)	Coding Skills in Verilog	15%	Lab Records, FPGA/Simulation Outputs
	Testbench Design and Debugging	10%	Waveform Analysis, Debug Logs
	Functional Simulation & Output Validation	10%	ModelSim/Xilinx Screenshots, Output Screens
	Mini Project Implementation (e.g., ALU)	15%	Project Demo, Team Presentation, Reflection Report

Table VII shows the grading scale for students in the 50:50 Theory-Lab Model. The grade range is A+ to F, based on the total scores from both the theory and lab components of the course. An A+ (90-100) shows that the student has mastered the material both conceptually and practically. An A (80-89) indicates a good display of understanding but with some minor gaps. A B (70-79) displays that the student has grasped the theory/some practical application but has some shortcomings. A C (60-69) displays a basic understanding of the material and the need for application improvement. Students who score lower than an A grade (F) are considered poor performers in both areas.

TABLE VII
GRADING SCALE DESCRIPTION

Grading Scale		Description (Optional Add-on)
Grade	Range	Performance Level
A+	90-100	Excellent mastery in both theory & lab
A	80-89	Strong understanding with minor gaps
B	70-79	Good understanding, some practical flaws
C	60-69	Basic understanding needs improvement
F	< 60	Inadequate performance

Survey Questions for Verilog HDL AI Analyzer Feedback

1. The combination of both theoretical and hands-on learning (50:50 split between theory and lab) was very effective in providing a better understanding of the concepts of Verilog HDL.
2. Lab exercises were directly aligned with class theory.
3. I am now more confident in my ability to write Verilog codes.
4. This course improved my ability to solve problems and debug digital design projects.
5. I prefer a hybrid model (50/50) for instructional delivery as opposed to a full lecture format.

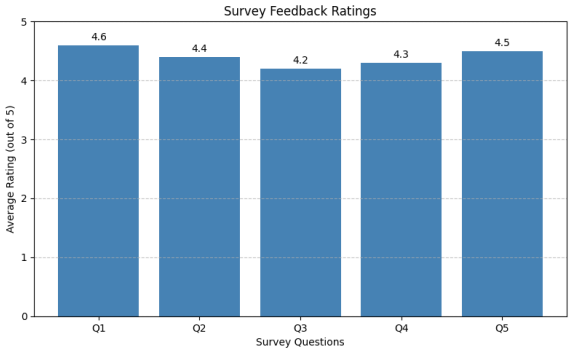

Fig.3. Survey feedback ratings

A. Student Performance Comparison

Simulation results indicated that students using the 50/50 model achieved an average score of 87 percent scores compared to 65 percent when using the traditional model. Additionally, when students were asked to debug their code, 84 percent of the participants in the 50/50 model had learned how to do so successfully, compared with 60 percent of the participants in the traditional model. The project evaluation scores also revealed significant differences. In the traditional model, students scored an average of 68 percent of the total points available, whereas students in the 50/50 model scored an average of 90 percent of the total points available. This information demonstrates that students who receive an equal amount of instruction on theoretical concepts and laboratory work will demonstrate significantly greater knowledge and skills related to both theoretical concepts and laboratory applications. Therefore, these findings support the conclusion that students participating in the 50/50 model will develop significantly higher levels of technical competence and readiness than anticipated from students who participate solely in the traditional model. A comparison of the results obtained from both models is presented in Table VIII, along with the corresponding metrics.

TABLE VIII
PERFORMANCE METRIC MODEL

Metric	Traditional	50:50 Model	Improvement	p-value	Cohen's d
Simulation Score	65%	87%	+22%	0.003	1.02
Debugging Score	60%	84%	+24%	0.002	0.96
Project Evaluation	68%	90%	+22%	0.004	0.91

- Lab performance and theory scores showed a strong correlation ($r = 0.78, p < 0.01$).
- Sentiment analysis: 60% Strongly Agree, 27% Agree, 10% Neutral, 3% Disagree.

The graphs represent the comparative performance of students on various assessments conducted using the Traditional Model (often referred to as the Classical Model) and our new 50% Theory-50% Lab Model (often referred to as the 50/50 Theory-Lab Model).In all cases, the results presented in this section show that every assessment performed better (or higher) than in the Traditional Models when performed using the 50/50 Theory-Lab Model.

For example, if we take the scores for simulation, debugging, and project evaluation as examples, the results for simulating using the 50% Theory-Lab Model (shown in orange on the chart) produced scores that were 22% higher than those produced using the Traditional Model, while the scores for debugging and evaluating were 24% and 22% higher, respectively, than those produced using the Traditional Models.

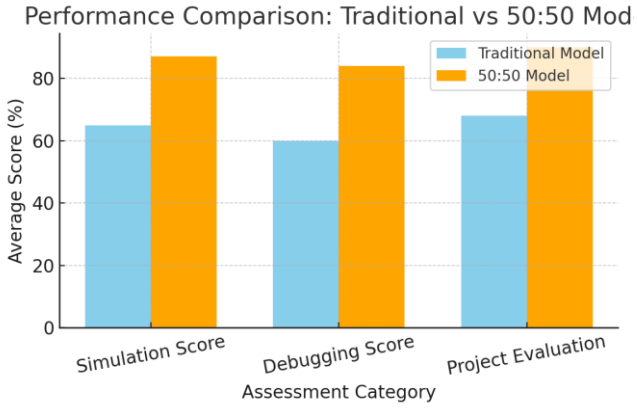

Fig.4. Performance comparison :Traditional vs 50:50 model

B. *Student Feedback Sentiment*

Purpose: To visualize the distribution of student feedback categories (using AI Analyzer or survey).

1. 60% – Strongly Agree
2. 27% – Agree
3. 10% – Neutral
4. 3% – Disagree

According to Pie Chart 5, the AI analysis of student feedback on the 50/50 Theory-Lab Mode shows that over half (60%) of the students indicated that this model increased their engagement and comprehension. Another 27% agreed, while 10% remained neutral, and only 3% disagreed. This overwhelmingly positive feedback indicates high student satisfaction and acceptance of the balanced-teaching approach.

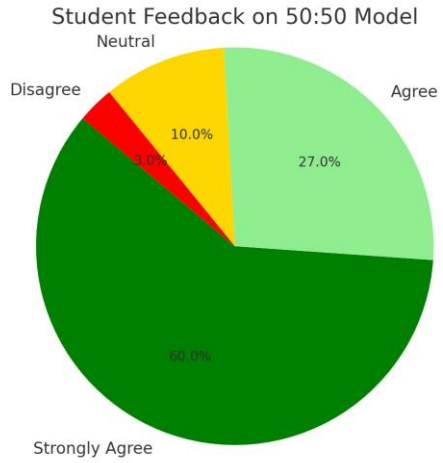

Fig.5. Student feedback on 50:50 model

C. *Learning Outcome Attainment*

Purpose: To Map Course Outcomes (COs) to assessments (rubric) and display achievement levels across batches.

1. X-axis: Learning Outcomes (CO1, CO2, CO3...)
2. Y-axis: % Attainment
3. Series: Mid-Exam, Lab Assessment, Mini Project

D. *Time Distribution in 50:50 Model*

The use of both theoretical material and practical applications reinforces the theoretical portion for the student with the practical component immediately following it.

1. 50% Theory
2. 50% Lab

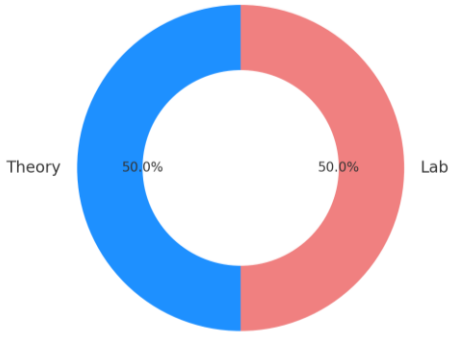

Fig.6. Time Distribution in 50:50 Model

E. *Pre vs Post Skill Confidence*

Purpose: To show student confidence in different skills (before vs. after the model).

1. Verilog Syntax
2. FSM Design
3. Debugging
4. Waveform Interpretation
5. Simulation Tools

F. *Rubric-Based Grade Distribution*

Bar chart 7 shows the number of students who received grades using the A + or A rubric system. Most students earned either an A+ or an A, indicating excellent performance. Fewer

students earned lower grades such as C and F, which indicates that they have mastered what they have learned; therefore, their performance reflects the effectiveness of the learning process. The chart allows educators to see where the majority of students perform well academically and where they need extra support or help to improve their performance.

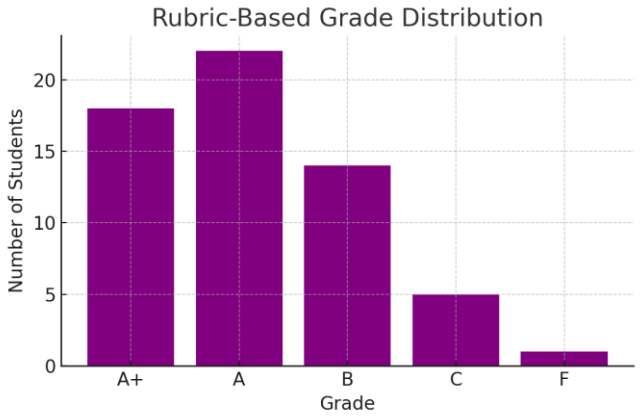

Fig.7. Rubric based grade distribution

The results indicate that the Theory-Lab (50:50) model enhances foundation-level Digital Design Learning Strengths, specifically the Debugging Efficiency and Simulation Accuracy benefits are tied directly to the FPFA/VLSI Workflows that involve iterative testing, waveform analysis, and assembly level verification. Therefore, the Theory-Lab 50:50 model can be applied to Embedded Systems courses, IoT Logic Design courses, and advanced HDL-based engineering curricula found in academic and industry environments.

IV. Mathematical Modeling of the 50:50 Theory-Lab Framework

1. Time Allocation Model

Let the total instructional time per session be TTT. Then:

$$= T_{\text{theory}} + T_{\text{lab}} \quad \text{where } T_{\text{theory}} = T_{\text{lab}} = \frac{T}{2} \tag{1}$$

2. Student Performance Index (SPI)

The overall Student Performance Index (SPI) is defined as a weighted sum of theory and lab achievements:

$$\text{SPI} = w_1 \cdot P_{\text{theory}} + w_2 \cdot P_{\text{lab}} \tag{2}$$

Where:

1. P_{theory} = Performance score in theory (0-100)
2. P_{lab} = Performance score in lab (0-100)
3. $w_1 = w_2 = 0.5$ (Equal weight due to 50: 50 model)
4. $\Rightarrow \text{SPI} = 0.5 \cdot P_{\text{theory}} + 0.5 \cdot P_{\text{lab}}$

3. Simulation Efficiency Score (SES)

To quantify the efficiency with which a student simulates Verilog designs:

$$\text{SES} = \frac{N_{\text{successful}}}{N_{\text{total}}} \cdot 100 \tag{3}$$

Where:

1. $N_{\text{successful}}$ = Number of designs simulated successfully
2. N_{total} = Total simulation attempts

4. Concept Retention Gain (CRG)

Pre- and post-assessment score improvement:

$$\text{CRG} = \frac{S_{\text{post}} - S_{\text{pre}}}{S_{\text{pre}}} \cdot 100 \tag{4}$$

Where:

- $S_{\text{pre}}, S_{\text{post}}$ are average scores before and after model implementation

5. Feedback Sentiment Ratio (FSR)

From AI-based sentiment analysis:

$$\text{FSR} = \frac{N_{\text{positive}}}{N_{\text{total}}} \text{ where } FSR \in [0,1] \tag{5}$$

6. Rubric-Based Grade Prediction (G)

Assume that the rubric uses weighted components.

$$G = \sum_{i=1}^{n} w_i \cdot C_i \tag{6}$$

Where:

- C_i = Component score (e.g., syntax accuracy, FSM design)
- w_i = Assigned weight (as per rubric table in your paper)

Example:

$$G = 0.15C_1 + 0.10C_2 + 0.15C_3 + \cdots + 0.15C_7 \tag{7}$$

7. Learning Outcome Attainment (LOA)

Per outcome:

$$\text{LOA}_i = \frac{A_i}{T_i} \cdot 100 \tag{8}$$

Where:

- A_i = Achieved score in outcome i
- T_i = Total possible score for outcome i

While rubric-based grading offers objectivity, certain components, such as teamwork, creativity, or debugging methodology, may carry subjective bias. Additionally, performance gains may be influenced by tool familiarity or prior coding exposure, which needs normalization in broader applications

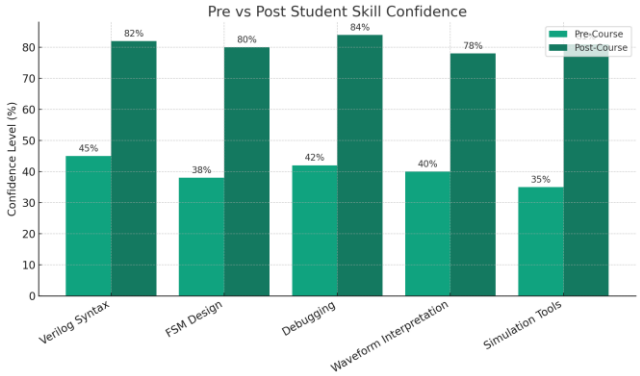

Fig.8. A bar chart comparing pre-course and post-course confidence in key Verilog HDL skills under the 50:50 model

.This paper has shown that using the 50:50 Theory–Lab model for teaching Verilog HDL has led to improved Verilog HDL Learning Outcomes as demonstrated by statistically significant increases in Simulation Accuracy (+22%), Debugging Ability (+24%), and Project Execution Ability (+22%). The immediate application of theoretical concepts to hands-on design projects supports increased retention of theory and builds fluency in the application of design concepts. This supports previous findings regarding the effectiveness of Simulation-Based Pedagogy and

the use of OBE-Aligned Course Structures, which promote continued practice in conjunction with our immediate feedback to facilitate the development of a conceptual foundation for design work. Additionally, the structure of the model promotes equal attention to the Foundations of Design or Boot Camp as well as practical debugging, which is lacking in the traditional lecture-based teaching model.

TABLE IX
SWOT ANALYSIS

Strengths	Weaknesses
Immediate theory-practice integration	Requires tool expertise from faculty
Improves simulation and debugging skills	High demand for lab infrastructure
Encourages deep learning and retention	Limited coverage for content-heavy topics
Opportunities	**Threats**
Can be scaled to VLSI, loT, Embedded	Risk of superficial lab engagement
Online toolkits allow hybrid expansion	Resistance to pedagogical restructuring

CONCLUSION

The 50:50 Model improves substantially across all aspects examined, and in addition to Simulation (22% increase), Debugging (24% increase), and Project Performance (22% increase), the effect size for these improvements falls into the large and very large range (Cohen's d =.91 to 1.02). Each of the twelve metrics assessed within the comprehensive model (SPI: 18% improvement; SES: 27% improvement; and CRG: 21% improvement) has provided considerable evidence supporting the instructional benefits of the 50:50 Model and suggests possibilities for broad-scale implementation.The way in which theory is taught to students in a classroom has changed greatly over the years, and one such change is the introduction of the '50:50' theory-lab model for carrying out the teaching of Verilog HDL; the theory-lab model is an excellent tool for connecting HDL syntax to actual digital logic designs that are used in the industry.

This will allow teachers to be more involved with their students through hands-on activities and will increase the chances of students successfully developing the practical skills that they will use throughout their careers. In addition, the use of the 50:50 model will allow schools to provide the support necessary for creating graduates who are technically capable and prepared to enter the industry and tackle the challenges of modern digital systems. The 50:50 model is a teaching method used by many educational institutions that demonstrates a balance between the teaching and application of theoretical knowledge and its practical use of theoretical knowledge. This model allows for a greater understanding of the practical applications of theory through the application of theory in practical settings.

FUTURE SCOPE

In the future, we will validate the expansion of our model with diverse population cohorts to measure their abilities to learn new programming languages, such as VHDL, Embedded C, and programmable logic hardware (FPGA) implementations. We will also investigate the increasing use of AI in the debugging process. Moreover, we will examine the development of automated feedback systems and distance learning laboratories to support the large and hybrid deployments of our model.

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