

Collaboration of UG-PG Learners for Enhancement of Digital Design Verification Aptitude Using PBL Methodology

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Abstract: The courses like system Verilog, VLSI Design Verification & Testing and Digital Signal Processing are considered for this activity. Delivery of these courses is centralized upon development of verification environment to identify and fix the bugs in DUT (Design Under Test). This is achieved by generating test vectors through programming. The proposed work binds three levels of learners namely UG, PG and course owner by attaining proficiency in verification of digital design. The methodology is implemented in three major phases namely design of modules, preparation of verification plan and development of verification environment and coverage analysis. Project based learning (PBL) is used to implement the proposed methodology. PBL improved student's attainment by 15% as compared to previous year in VLSI Verification course. The average marks attained by both UG-PG is 79%. This also helped students to grab placement opportunities in VLSI verification domain. Also students experienced the industry culture of various teams working on single project.

Keywords: PBL, Verification plan, Attainment, VLSI verification, Collaboration, UG-PG, DSP

1. Introduction

In traditional teaching learning method there is one way communication from teacher to students but, student's teacher communication has become very rare except students show some interest. In traditional method delivery of knowledge to students does not guarantee that all will be received by students. The effective learning happens only when two way communication takes place

between students and teacher. To enhance participation of students in learning and gain knowledge, many active learning techniques comes into existence. The PBL is one among various active learning techniques works on the mantra called "Learning by Doing".

Especially in academic, effective learning takes place when discussion happens at same age group or small age difference group as compared to the group of members where age difference is significant among teammates. The PBL provides a platform where same age or less age difference groups comes together to express their views on the topic.

(Intel tech 2012) Described concept of PBL inquiry in learning, benefits of PBL, Transformation of traditional classroom using PBL and various challenges faced by students and teachers in traditional teaching learning method and activity based teaching learning method. Also described challenges in implementation of PBL. (Shaban, 2018) Described PBL implementation and challenges faced by primary school pre service teachers. However, most of these aspects applicable to engineering graduates and teachers also. The challenges related to teachers, students, curriculum, schools, parents are described. (Barbara et al., 2017) In current education research profession these competencies are usually called as "21st century skills", "deeper learning," or "college and career readiness skills." The NRC committee clarified these concepts by defining "21st century learning competencies" as the "transferable knowledge" and "skills" that are produced through deeper learning processes. The aspects of learning for transfer, novices and experts has been detailed. Along with these research details, The PBL implementation describes the way how context contributes, investigate the effectiveness of implementation of various models for professional development of PBL, focus on the use of technology, deliverable, instructional strategies, study the link between

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teacher's beliefs and implementation, develop reliable measures of intra and interpersonal competencies.

PBL effects on math and literacy skills, and also focus on underserved student populations.(Nizwardi et al.,2017)Discussed seven steps of PBL model to improve student's competencies and learning activity, formulation, designing projects to solve real time problems and team work.(Douglas,2000) given detailed steps and 6A's for effective execution of PBL. (Margaret ,2011) This article provides a review of research happened on effective implementation and productive outcome of PBL from 2000-2011 at preschool level. This includes academic improvement in education, learning ability of students and teachers. This paper initially provides information on PBL and their historical context. Next, the reviewer combined various aspects emergent in the literature including attitudes of student and teacher, growth in academic, overall development of students and teachers and finally recent trends in project-based learning with specific student subgroups.(Arwizet K,2018) This paper provides collaborative learning models using PBL. This gives the comparison study of students learning related to energy conversion machine course and thermodynamics using PBL technique and conventional technique.(Joseph S,Book) Provides an idea of better design and implementation of PBL in consideration with many aspects of teaching learning methodologies and student and teacher centric challenges. (Zancul et al.,2017) Demonstrated the product development of undergraduate course based on a project-based learning (PBL) perspective. The PBL has been elaborated as effective teaching learning method in engineering education. Also discussed some fit falls of PBL implementation and shown improvement in students learning in terms of academic, body language and personality development. This paper demonstrated the collaboration of different interdisciplinary teams to provide complete solution.(Mohd Shafie et al.,2005) Defined the implementation of PBL for computer programming course and also discussed problems faced during implementation of PBL. At the end suggested some points for the improvement of PBL. (Hetty and Wendy, 2011) Identified and described various guiding instructions to design and implementation of problem based learning, evaluation & monitoring strategy in the context of pre and in service teaching profession.(Utku Köse 2010)Improved students learning in Web design and programming course with PBL. The web system is designed under PBL activity. The PBL also inculcates diversity of characters in a team from various academic levels to experience the industry culture during academic. This makes students to aware of industry working culture and takes little effort to get

adjust to industry environment after their graduation. But the fact that PBL alone cannot serve the purpose unless proper guidance, monitoring and controlling the PBL activity for effective outcomes. There comes the role of teacher for effective planning, implementation and monitoring of PBL activity. In this process teacher has to facilitate students technically and motivate them to reach their goal.

The proposed work explores the new aspects of PBL by collaborating undergraduate and post graduate students to share knowledge and develop industry culture in academic. The PBL technique is applied for undergraduate courses such as System Verilog, Digital Signal Processing and post graduate course VLSI Design, Verification and Testing, Advanced Digital Signal Processing. The respective courses from UG and PG were selected due to close match between course content of these courses. Though there is close match between course contents, the depth of delivery of course is different for UG and PG. This factor motivates to the idea of collaboration of both UG PG students through PBL. Organisation of this paper is as follows: section 2 deals with methodology, Section 3 describes the results and discussion and section 4 gives the conclusion and challenges faced during implementation of PBL.

2. Methodology

There are three levels of learners are associated with proposed methodology. UG, PG and course owner. The main role of course owner is to act like a facilitator for effective implementation of PBL. The conceptual methodology of proposed PBL is shown in figure 1. Since mentioned courses in section 1 have emphasis on verification of designed system rather than formulation and designing of system based on problem statement. Hence more stress is given on verification hence, designed & buggy digital systems are given as problem statement to students groups. These systems are formulated and designed by course owner and some bugs are added deliberately at deep modular level. This requires skilled engineer to identify the bug and fix it before forward the design for fabrication.

The methodology flow of proposed PBL is shown in figure 2. UG and PG students are divided into groups separately. Each heterogeneous group has all levels of learners like slow, medium and fast learners with different band of earlier CPI. This kind of group formation helps slow and medium learner to actively participate in PBL since everyone is representing part of the work individually.

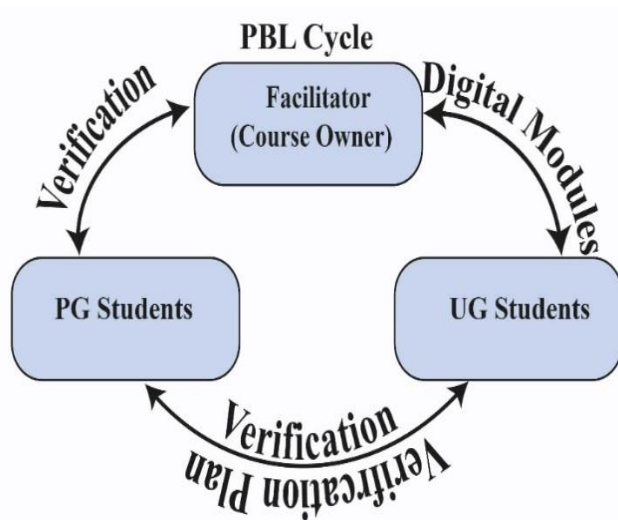


Figure 1: Conceptual methodology of proposed PBL

The main functions included in PBL are as follows

Table 1. Methodology of proposed PBL activity

Sr. No	Particular	Task	Responsible person
1	Problem Statement	Design of Systems	Facilitator (Course Owner)
		Redesign of Systems based on feedback from verification plan team/validation team	
		Demonstration of systems	Target Audience: UG PG students
2	Preparation of Verification Plan	Understanding of Problem Statement	UG Students
		Modularization of system	
		Detailed input output information of each module	
		Identification of test vector for each	

		module and system as a whole	
		Set of test cases to be generated	
		Corner case test vectors	
		Golden Values	
		Presentation	Target Audience: Associated PG students and facilitator
3	Writing Verification code	Selection of coding style	PG Students
		Reusable Test bench	
		Physical generation of various test vectors	
		Test vector to verify functionality of critical block	
		Proper timing signal generation	
		Comparison of results with golden values	
4	Validation of Design	Code coverage Analysis	PG Students
		Function Coverage Analysis	
		Modification in test bench	
		Reapplication and analysis	
		Coverage report	

		preparation	
		Discussion with facilitator & UG students	
		Feedback to change verification plan to UG students	
		Repeat the steps 3 & 4	
		Feedback to change design	
5	Tap-out	Manufacturing of chip	Physical design

The table 1 supports to understand the complete methodology flow of proposed PBL. The table 1 consists of functions of each level of learner at each phase in PBL. Table 1 also depicts micro level tasks at each phase along with the team which is going to perform the task. The formulation of problem statement and design is done by course owner and only pseudo information of designed module is given to UG and PG students. Both UG PG students associated to the particular project brought together and discussed on given module. UG students prepared a verification plan. During preparation of verification plan many aspects have been considered and are listed in 2 phase of table 1. The functions of PG students is to write verification test bench based on verification plan and verify the design with all aspects by analysing code coverage and functional coverage. The code coverage is quantitative analysis of execution of each line of code written in DUT & verification model to assure that DUT will function satisfactory in all scenario. If % code coverage not attained, PG students have to modify the test bench. After modification, if code coverage is attained but functional coverage not, then discussed results with UG students and instructed to modify the plan. The functional coverage provides quantitative analysis of verification of all features implemented in DUT. This gives information about the feature which is/are not considered in verification and may have bug in the design. If functional coverage is not attained then the coverage results are discussed with whole team and facilitator to change the design.

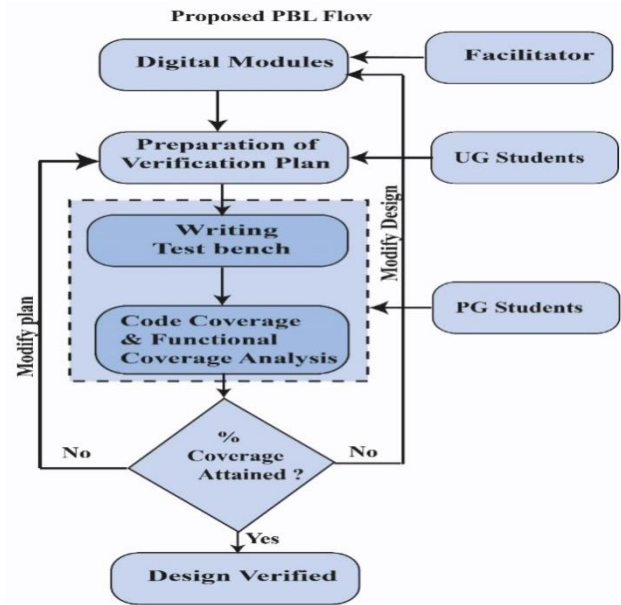


Figure 2: Flow of implementation of PBL

3. Results and discussion

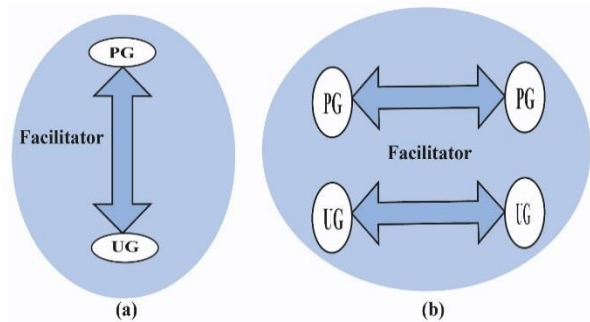


Figure 3: Vertical and horizontal flow of knowledge

Figure 3 shows bilateral/trilateral participation and knowledge flow in this activity. A team of UG –PG has same project and is been divided into two major parts. As mentioned in table 1 verification plan is prepared by UG team and verification function is done by PG team. UG team discuss among themselves and also with facilitator if required and prepare a verification plan. During this process the knowledge shared between members of same team(Horizontal) is shown in figure 3b. Figure 3a shows, once verification plan is prepared, is shared to PG team for verification process as per the plan(Vertical flow of knowledge). PG team write verification code as per the plan provided by UG team in consultation with all members of their team as shown in figure 3b(Horizontal). If 100% verification of DUT is not achieved, then PG team communicates with UG and discuss with facilitator

to take necessary action to achieve complete verification of DUT as depicted in figure 3a. The role of facilitator is to assist both teams to complete their task effectively.

The figure 4 shows sample of verification plan prepared by UG groups on Booth Multiplier and First in First out (FIFO) respectively. Figure 5 shows coverage analysis after verification of modules by PG groups. This shows the values generated for verification of design and verification status. If design functions properly the tool generates the status as *success: match*, else gives failure message.

This activity has contributed significantly in students learning and attainment of course outcomes of UG as compared to previous year. Also PG students CO attainment is observed as remarkable.

Figure 6a depicts COs attainment of last two years of UG students. This shows improvement in attainment of COs of the courses. The average marks obtained by UG students in 2017-18 is 74% and in 2018-19 average marks is 79.2%. Figure 6b shows the COs attainment of PG students of 2018-19. The average marks obtained by PG students is 79.1%. This course is introduced for PG in 2018-19 curriculum hence no prior data is available for the comparison.

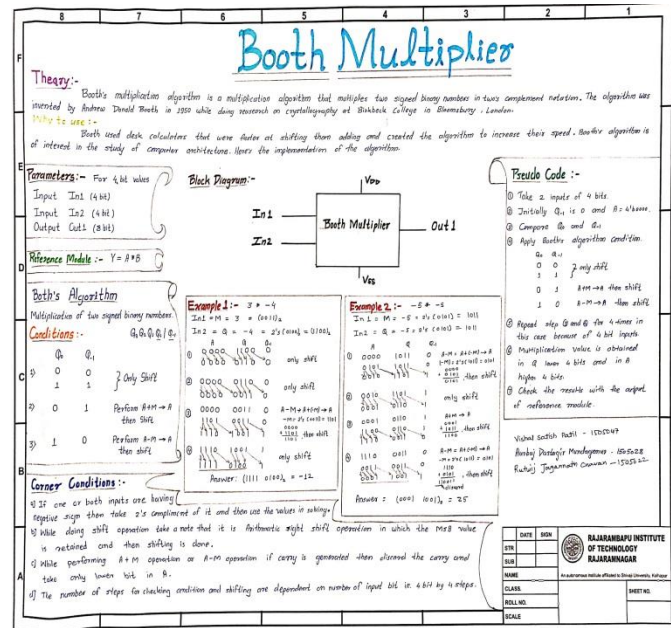
The attainment is calculated based on equation 1

$$\text{Attainment \%} = (x/y) * 100 \text{ -----(1)}$$

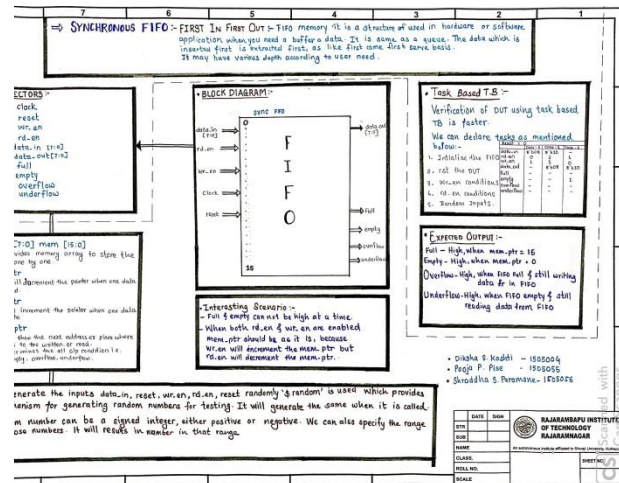
x = Count of Students $\geq$ to Threshold %

y = Total number of Students Attempted.

Threshold set for UG and PG attainment calculation is 60%.



(a)

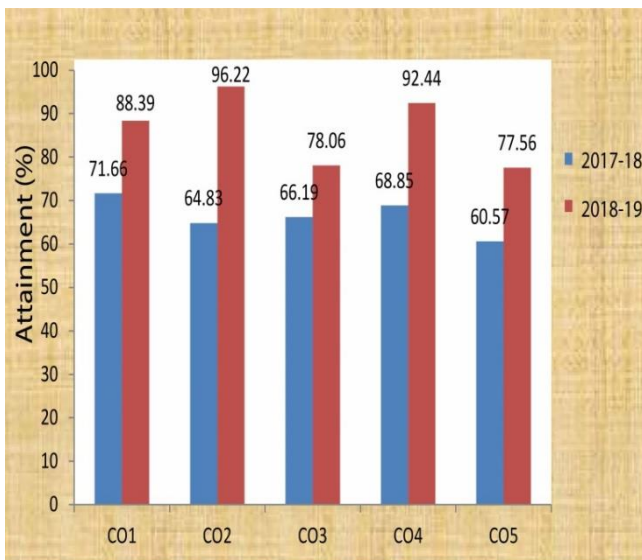


(b)

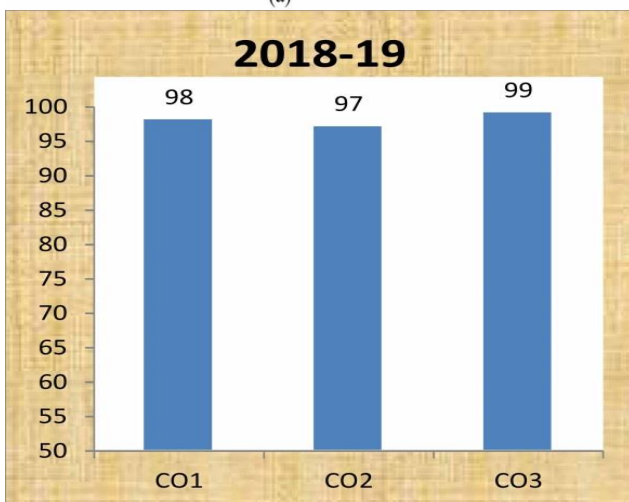
Figure 4: Sample Verification plans

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*****
Successfully generated values on X, Y
Generated Value of X=0001, Y=3
DRIVER sent values to SCOREBOARD as input X= 1, Y= 3
DRIVER sent values to DUT as input via INTERFACE X= 1, Y= 3
Output of DUT sent to MONITOR is      X= 1, Y= 3, Z= 3
Values sent from MONITOR to SCOREBOARD is X= 1, Y= 3, Z= 3
SUCCESS: Match
145 value pkt1.X= 1, value pkt2.X= 1, value pkt1.Y= 3, value pkt2.Y= 3,
value pkt1.Z= 3, value pkt2.Z= 3
*****
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Figure 5: Verification results



(a)



(b)

Figure 6 (a). Comparison of attainment of two academic years of UG (b). One academic year of PG

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PBL Feedback Form

We would appreciate if you could take a few minutes to share your opinions with us so we can serve you better.

Date: 18th April 2018 Instructors: Prof. Sachin M Magdum
Prof. Randhir J. Patil

	Strongly disagree	1	2	3	4	5	Strongly agree
1. Rate the process of implementation of PBL.							
2. The activity was well paced within the allotted time							
3. The instructors were good facilitator							
4. Do you feel this activity helps for your development							
5. Would you recommend such activity for all courses of UG PG							
6. Rate your learning of VLSI verification course with this activity							
7. Process of team formation provides balanced team							
8. Was there flow of knowledge between UG PG							
9. Do you feel problem statements were challenging							

10. Please rate the following:

	Excellent	Very Good	Good	Fair	Poor
a. Facilities	☒	☐	☐	☐	☐
b. Assistance	☒	☐	☐	☐	☐
c. Knowledge gained	☒	☐	☐	☐	☐
d. Team work	☒	☐	☐	☐	☐
e. The activity overall	☒	☐	☐	☐	☐

11. What are the most helpful points about this activity?
The activity helped me to understand working in team projects. Also it helped me to understand fundamentals with quick guidance from seniors.

12. Suggestions to improve this activity
Need more hours.

Name and Signature
Randhir J. Patil

nit Kasegaon Education Society's
Rajarambapu Institute of Technology, Islampur
 Department of Electronics and Telecommunication

PBL Feedback Form

We would appreciate if you could take a few minutes to share your opinions with us so we can serve you better.

Date: 18th April 2018
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Instructors: Prof. Sachin M. Magadum

1. Rate the process of implementation of PBL. Strongly disagree 1 2 3 4 5 Strongly agree

2. The activity was well paced within the allotted time. 1 2 3 4 5

3. The instructor was a good facilitator. 1 2 3 4 5

4. Do you feel this activity helps for your development. 1 2 3 4 5

5. Would you recommend such activity for all courses of UG PG. 1 2 3 4 5

6. Rate your learning of VLSI verification course with this activity. 1 2 3 4 5

7. Process of team formation provides balance team. 1 2 3 4 5

8. Was there flow of knowledge between UG PG. 1 2 3 4 5

9. Do you feel problem statements were challenging. 1 2 3 4 5

10. Please rate the following:

	Excellent	Very Good	Good	Fair	Poor
a. Facilities	☐	☒	☐	☐	☐
b. Assistance	☐	☒	☐	☐	☐
c. Knowledge gained	☐	☒	☐	☐	☐
d. Team work	☐	☒	☐	☐	☐
e. The activity overall	☐	☒	☐	☐	☐

11. What are the most helpful points about this activity?
Helped me to know about leadership responsibility.
Some of unknown fundamentals were reviewed which will help me in my internship.

12. Suggestions to improve this activity
More weightage must be more to read more time.

Name and Signature: Randhir J. Patil
Periva G. G. G. G. G.
18/04/2018

Figure 7: Sample feedback forms of UG and PG students

Rate	Q 1	Q 2	Q 3	Q 4	Q 5	Q 6	Q 7	Q 8	Q 9
1	0	1	0	0	1	0	0	0	0
2	0	6	1	2	2	3	0	2	0
3	8	15	12	10	11	14	3	9	2
4	8	19	17	24	22	28	26	26	1
5	40	15	26	20	20	11	27	19	7
Total Responses	56	56	56	56	56	56	56	56	56

Table 2: Students responses about activity Q1-Q9

The figure 7 shows the sample feedback from by students of UG and PG. Table 2 & 3 shows the overall students responses as per their level of satisfaction about the activity in terms of rating. This is the formal assessment of activity. For the assessment of UG students

rating taken by team member of PG students of same project and PG students rating is done by facilitator.

Q10	Facilities	Assistance	Knowledge Gained	Team Work	Overall Activity
Excellent	19	18	21	25	22
Very good	21	22	24	22	19
Good	13	15	8	3	11
Fair	2	1		2	3
Poor	1	0	1	1	1
Responses	56	56	56	53	56

Table 3: Students responses about activity Q10

4. Conclusions

The proposed PBL methodology significantly contributed to change in course outcomes attainment and results discussed in section 3. The free flow of knowledge in vertical and horizontal direction is observed. This also helped students to grab internship and placement opportunities. Placement, Internship and higher studies opportunities grabbed by students in VLSI verification domain of UG PG students is as shown in figure 8.

Some PG students got selected for internship in Linked Loops Pvt. Ltd. Pune which is working on embedded and VLSI domain. The feedback which we got from this industry was as follows i. Students are well-versed with HDL language ii. Familiar with verification methodology iii. No need to train students in this area.

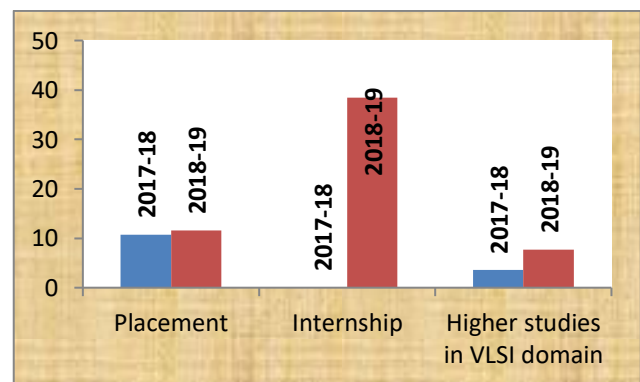


Figure 8: Placement, internship and Higher studies in VLSI domain.

The proposed methodology has showed qualitative improvements in student's skills such as team synchronization, interpersonal skills and knowledge sharing. Apart from many positive aspects, there are some

challenges also to be addressed during implementation of this methodology. Some of them are as follows. i. Identification of suitable problem statement ii. Expertise in design of module iii. Placement of bugs in designs iv. Curriculum time constraint v. Initial synchronization of UG-PG students. vi. Monitoring of projects. vii. Motivation of students. Overall this improves students learning ability hence can be extended to various courses of UG-PG to inculcate industry work culture during their education.

Acknowledgement

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