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Teaching Fundamentals of Microelectronic Technology Using Test Chip

Sudhir Chandra[1], Saakshi Dhanekar[2], Jaidrath Yadav[3], Dalesh Kumar Sahu[4], Anudeep Singh[5]
[1]Electronics and Communication Department, Bennet University, Plot No. 8-11, Tech Zone-III, Greater Noida-201310, UP, India
[2,3,4,5]Centre for Applied Research in Electronics, Indian Institute of Technology Delhi, Hauz-Khas, New Delhi, 110011, India
[1]sudhir.chandra@bennett.edu.in
[2]sdhanekar@care.iitd.ac.in

Abstract: In this work, we present an innovative approach to provide training to undergraduate and postgraduate students in the area of microelectronics technology through test chip design, fabrication and testing. A large number of academic institutions across the world do not have device fabrication facilities at their disposal. In such cases, imparting even basic training to the students in the area of microelectronics technology is severely restricted. In the work presented here, a test chip, based on a generic bipolar process, has been designed and fabricated. The test chip contains various test structures through which process parameters (such as sheet resistance of diffused layers, contact resistance etc.) can be measured. In addition, the chip has a few diodes and bipolar junction transistors of different designs and dimensions. The devices were packaged in a standard integrated circuit header but with a transparent cover to enable optical viewing. The devices and test structures were characterized and the measured parameters were correlated with the processing parameters. The electrical measurement on these structures together with processes used in fabrication and the visual observation under an optical microscope is helpful to students in developing better understanding of the intricacies of device fabrication.

Sudhir Chandra
Electronics and Communication Department, Bennet University, Plot No. 8-11, Tech Zone-III, Greater Noida-201310, UP, India
sudhir.chandra@bennett.edu.in

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1. Introduction

Semiconductor devices have entered all walks of life in today's world. There is hardly any domain of human activity where these devices are not being used advantageously. Examples are: communication, entertainment, computing, medical diagnostics, imaging, banking, internet, defence, space, energy, lighting, education and many more sectors. Over the past five to six decades, the complexity of electronic chips has been steadily increasing whereas the cost of gadgets having these chips is progressively coming down due to remarkable progress in chip making technologies and associated developments in material science and engineering.

Today, a cell phone has almost same degree of computing and communication power that was available in the main-frame computers, not too long ago. The rapid pace of development in electronic circuit design and manufacturing, communication technologies, instrumentation and computer science and engineering disciplines has led to the emergence of new branches in engineering education and a need for continuous improvement and revision of syllabi. The need forincorporating sound practical training in the curriculum of engineering education was always the necessity for the engineers to be job-ready. This has become more and more critical in recent times.

The practical training to students in the area of electronics and microelectronics can be broadly classified in three categories namely (i) hardware electronics circuit design, assembly and testing using breadboard-printed circuit board (PCB) approach (ii) circuit design, simulation, testing and analysis using software tools. (iii) device fabrication and related subjects. The lab and infrastructure related requirements for the first two categories of practical training are vastly different from those for the third category. While sufficiently advanced training in the first two categories can be provided with the resources available with well-established academic institution, the training in microelectronic device fabrication related subjects requires an infrastructure of very different dimensions and magnitude. To establish, maintain and run a semiconductor device fabrication facility, even on a very modest scale without having high-end clean room, is beyond the resources available at most of the Educational Institutions. The concept of using foundry services for getting the chips fabricated has greatly bridged the gap that existed in training the students in the vital area of chip design and testing. However, some exposure to basics of devicefabrication and "seeing" the actual chip is still a dream for most of the students, even in fairly highranking Universities and Colleges. In the present work, we have made an attempt to explore how this gap can be partially bridged, using a test chip based approach for students training.

The organization of the present work is as follows:

(i) The methodology underlying the present work ispresented.

(ii) The details of test-chip design and fabrication steps are outlined.

(iii) Results on electrical characterization and measurements of various test structures and devices on wafer level are presented

(iv) The wafer dicing and chip packaging. This was outsourced to a Company. Here it may be mentioned that the final lid on the package was a glass plate of matching size which was fixed using glue. This feature enabled viewing the chip under microscope for students training

(v) The results, discussion and conclusion.

2. The Methodology

As a first step, the process sequence to be followed for chip fabrication was frozen. This was based on the unit processes available in the lab which could be readily adopted without much further experimentation. The next step was to identify important test structures and devices which can be used for characterization of processes carried out in chip making and also correlate the device performance with the process parameters chosen. The next critical step was selecting the chip floor plan, the chip size, the overall layout dimensions on artwork keeping in mind the limitations in mask making, wafer dicing and packaging. In the following Sections, details of these will be presented.

The Process Sequence

The process sequence used in the fabrication is summarized in Table 1. It employed four masking steps for defining (i) boron diffusion area (ii) phosphorus diffusion area (iii) contact windows and (iv) metallization pattern [1-3]. The starting wafers were: 2-inch diameter, n-type, 1-10 ohm-cm resistivity having (100) orientation. Accordingly, the process sequence could provide NPN bipolar junction transistor.

The Artwork Preparation and Mask- making

The masks were designed using Intellicad and the artworks were generated by laser writing process on photosensitive plastic sheets. The laser writing process was outsourced to a local vendor which had facilities to print line widths down to 300 µm. The artwork size was 100 cmby 100 cmand these were made 20 times larger than the actual size. These were then transformed on to photosensitive glass plates of 2.5" x 2.5" size using First Reduction Camerato obtain final working masks. All the masks were "Bright Field Masks". The reduction ratio was 20x. Contact mask aligner was used for photolithography process. The layout of complete wafer is shown in Fig. 1.

Test Structures and Devices

The chip contained: bridge and Van der Pauw test structures for sheet resistance measurement, Hall effect measurement structure, Kelvin Bridge structure for contact resistance measurement, diodes and

transistors of different shapes and size [4]. The masks were generated using First Reduction Process only in a single reduction step (without using a Step and Repeat Camera). This allowed us to place different chips on a single wafer. However, if the masks are made in a more professional mask making facility which uses a Step and Repeat Camera also, one would get all the identical chips on a wafer. Use of a wafer stepper in photolithography process may allow different designs to be made on the same wafer.

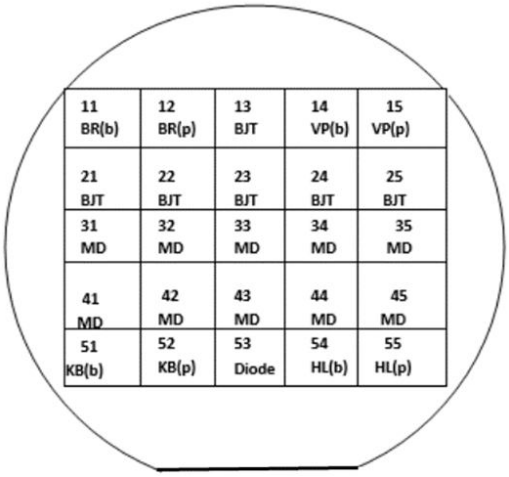

Fig. 1 Floor plan of the test chip. Chip No. 31-45 are identical chips having various test structures and devices for packaging on 40-pin header. Other chips contain single device or test structure: BR: Bridge test structure; VP: Van der Pauw test structure, KB: Kelvin Bridge test structure; HL: Hall Effect test structure; BJT: Bipolar junction transistor.

However, this was excluded from consideration as wafer stepper was not available in our process lab and also our aim was to keep the process as simple as possible.

Accordingly, two types of chips were included in the layout. (i) Chips with multiple test structures and devices. In all, there were 10 chips of this kind, all identical. These will be referred as multiple device chips or MDC (ii) Chips which has only one type of test structure or device and these will be referred to as Single Device Chip or SDC. The size of both of these chips was identical: 5 mm x 5 mm. The significant difference in the two types of these chips was in the size of bonding pads. The SDC has large bonding pads (2 mm x 2 mm) whereas MDC had bonding pad size of 200 micron x 200 micron. The underlying idea was that in case the wafer dicing and wire bonding steps (to be carried out at an Industry) do not materialize satisfactorily, we would dice the wafers in the Lab and package SDC and do wire attachment using silver epoxy, as bonding pads were of large size. This would allow us to salvage significant part of the wafer and allow us to test several test chips and devices. Both SDC and MDC were packaged and tested.

Fabrication Steps

The details of recipes used in fabrication process are given in Table 1. Optical images of the processed wafer and various structures are shown in Fig. 2. Different test structures are shown from Fig. 2(a) to Fig. 2(d) whereas diodes with different area are shown in Fig. 2(e). Bipolar transistor having different designs are presented in Fig. 2(f) to 2(h). The picture of full wafer is shown in Fig. 2(i). The multiple device chip (MDC) is shown in Fig. 2(j).

Measurements

Table 1 Process sequence for fabrication

S. No.	Process Step Details
1.	Wafer specification and cleaning: n-type, (100), 1-10 ohm-cm, standard cleaning
2.	Thermal oxidation: 1 micron thick SiO_2, dry-wet-dry
3.	Photolithography:Mask M1 for boron diffusion
4.	Boron diffusion using planar solid Boron+ source: Pre-dep for 1,2,3 hrs at 950°Cand drive -in recipe : dry (10 min), wet (30 min) and N_2 annealing (3,4 hrs) at 1100°C
5.	Photolithography: Mask M2 for phosphorus diffusion
6.	Phosphorus diffusion: Pre-dep: 1 hr at using planar source at 950°Cand drive -in recipe : dry (10 min), wet (30 min) and N_2 annealing (90 mins)at 1100°C
7.	Photolithography: Mask M3 for opening contact windows
8.	Oxide etching : In buffered HF for opening contact windows
9.	Aluminium deposition : by thermal evaporation for metal contacts, thickness: 1 µm
10.	Photolithography: Mask M4 for patterning PR on aluminium
11.	Metal etching : In Al etchant for etch exposed aluminium

Optical images of the processed wafer and various structures are shown in Table 1 Electrical measurements on wafer level were performed using a wafer prober (Ecopia). Fordiode and transistor characteristics, Keysight I-V E49880A measurement setup was used.

Results and Discussion

First, we present the results of sheet resistance measurement. These were obtained from measurements on Bridge structure and Van der Pauw structures. For the bridge structure shown in Fig. 2(a), the sheet resistance was calculated from the measured values of voltage V between the two inner contacts while a current is forced between outer two pads. The corresponding equation is:

$$\rho_S = R \frac{w}{l} (1)$$

where, ρS is the sheet resistance (Ω / □□), R is measured resistance (V/I) and w, l are length and width of the bridge structure respectively. The sheet resistance measurement using Van der Pauw structure were also made. These do not require knowledge of dimensions of the structure and are less prone to errors. In our test chip design, these structures were included for boron and phosphorus diffusion process.

The sheet resistance value for born diffusion was measured to be 43 Ω/ □ □ and 50 Ω / □ □from Bridge test structure and Van der Pauw test structure respectively. For phosphorus diffusion, the corresponding values were measured to be 14 and 15 Ω. The measurements on Hall structure confirmed the doping type. The Hall voltage measurement along with resistivity measurement provides information on resistivity, doping density and mobility values. For these calculations, some estimate on the junction depth is needed. This simulation was also done using the experimental data on the process recipes followed in fabrication process. The details of these for estimation of carrier concentration and mobility values are not included in the present work. Using Kelvin structure, the contact resistance between metal and diffused layers was measured to be about 10^{-4} $m\Omega cm^2$ for both boron and phosphorus diffused areas.Measurements on diodes (emitter-baseand base-collector) were performed to check the integrity of the entire process sequence. The diode leakage current and the breakdown voltage were tested for this purpose and these were on expected lines. The details of these measurements are not included in the present work.

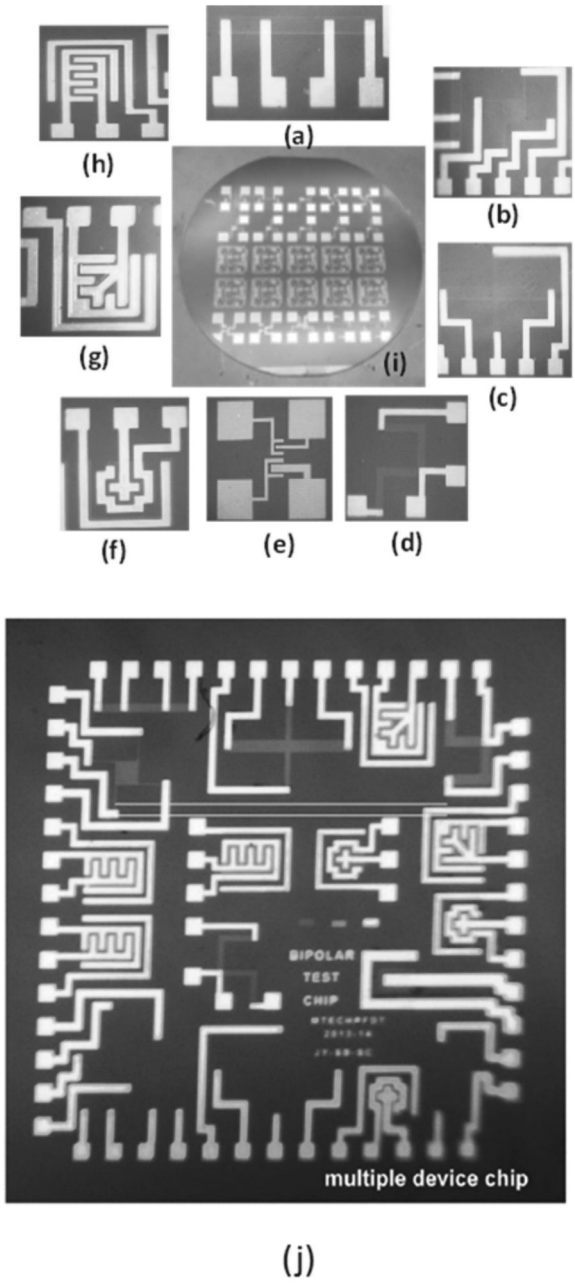

Fig. 2 Optical photograph of the fabricated wafer. (a) Bridge test structure, (b) Van der Pauw test structure, (c) Hall Effect test structure, (d) Kelvin cross bridge test structure, (e) Diodes, (f) – (h) bipolar transistors, (i) complete wafer with all structures and transistors, (j) multiple device chip

The bipolar transistor output characteristics were measuredin common emitter mode. The results are shown in Fig. 3.

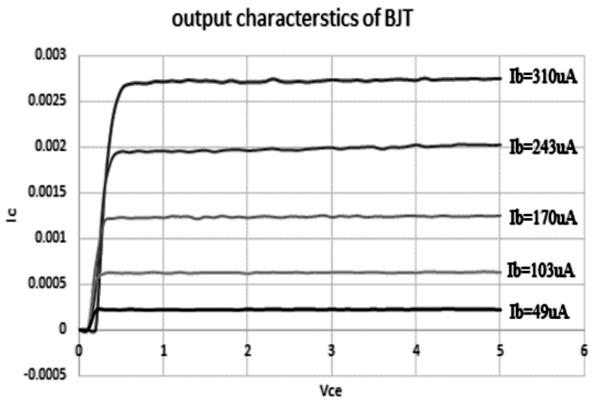

Fig. 3 Output characteristics of bipolar junction transistor in common emitter mode.

For the drive-in time of 9 hours for the base diffusion cycle, the current gain (β) was measured to 12. This is obviously too low a value for a good transistor. However, the process was not tuned and optimised to yield a high value of β. From the simple test structures included in this work, it is thus possible to obtain several parameters which are relevant to evaluate and correlate device performance and process monitoring. Sheet resistance measurements of diffused layers corresponding to base and emitter diffusion are characterized using Bridge structure and Van der Pauw structures. Coupled with Hall effect measurement, the average doping density, resistivity and mobility can be determined. If one is also able to simulate the process using a process simulator, the profile of dopants in diffused layers can also be obtained. From the point of view of imparting training to the students in microfabrication technology, a course can be designed to teach some aspects of integrated circuit fabrication to the students. Coupled with Lab experiments using the test chips, a fair amount of practical knowledge can be imparted to the students. In this work, we used glass covers on the package to enable students view the test structures and devices under optical microscope. Depending on the level of the course and the measurement facilities available in the Lab, one can select the individually packaged chips (SDC) for the experiments. A packaged chip containing the desired test structure allows the experiment to be conducted with minimum infrastructure without compromising the quality of learning. Many more test structures with advanced features can be included (e.g. Haynes Shockley's experiment for life time measurement) can be included. Similarly, a test chip based on MOS process can also be designed and fabricated. Several experiments can be designed based on MOS test chip.

A crucial issue in this entire exercise is where to get the chip fabricated and packaged? The answer to this critical question depends on the resources available at a particular location (University, College etc.). There are multiple options for this. One such option is that the chip is made at one of the well-established device fabrication labs of leading academic institutions within or outside India. The wafer dicing and packaging can be outsourced to a local company, as was done in the present work (Fig. 4). The chip having a single test structure (i.e. single device chip or SDC) can be wire bonded at any Lab using silver epoxy as it has large sized bonding pads. Another approach can be that a entrepreneur is involved and the chips making and packaging is completely outsourced. The vendor than markets these as experiments to academic institutions. Other options may also exist and needs to be explored.

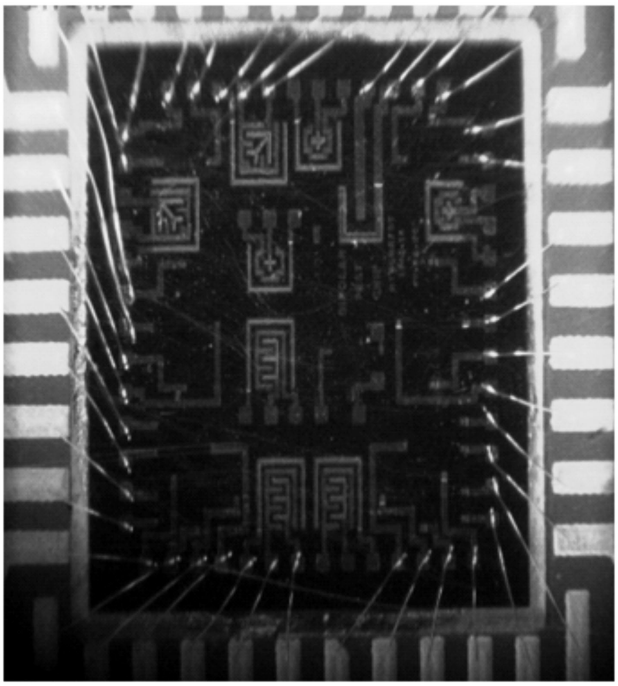

Fig. 4. MDC wire bonded to ceramic header

9. Conclusions

A test chip was designed based on bipolar transistor process, keeping in mind the constrains of the processing facilities and infrastructure available at the Microelectronics Lab of Centre for Applied Research in Electronics (CARE), IIT Delhi, where the entire work was carried out. It may be emphasized that the masks used in chip fabrication were also made at the same Lab using very modest mask making

facilities. The dicing of the processed wafer and wire bonding was outsourced to a Company. The measurements on test structures and devices were carried out. The chips had a glass cover instead of normal opaque metal lid. This feature enables viewing under an optical microscope to grasp several features of device making process. The central theme of the work was to explore and demonstrate that the practical training to the students in the area of Microelectronics Technology through test chips can be accomplished without having a processing Lab. The test chips made in the present work may be used as stand-alone experiment in courses being taught at undergraduate and postgraduate levels at Universities and Colleges.

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